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Investigation of Electromigration Reliability of Solder Joint in Flip-Chip Packages

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Investigation of Electromigration Reliability of Solder Joint in Flip-Chip Packages

by

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Dedication

To my family

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Investigation of Electromigration Reliability of Solder Joint in Flip-Chip Packages

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Electromigration related damage in solder bumps is one of the emerging issues resulting from the fast scaling-down of features in semiconductor packages. Although the electromigration phenomenon has been intensively studied on silicon level interconnect lines since the late 1960s, it is far less understood in solder bumps. Electromigration in solder joints can be quite different from that of the interconnects due to the differences in material systems and structures. This study addressed the solder joint electromigration and contained three major objectives.

The first objective of this study was to set up an effective experimental technique to examine the damage development and determine the time-to-failure in the electromigration tests. The structure and dimension of the flip chip solder bump is

very different from that of the chip level interconnect. Consequently, the traditional failure tracking method based on 2-point resistance monitoring is no longer able to provide real-time damage evolution information. A test system based on a Wheatstone bridge circuit was introduced. The technique showed the capability of detecting milliohm resistance changes and could track the interfacial crack growth induced by electromigration damage. Other aspects of the experiment, such as temperature and current distribution inside the test structure, were also examined so that proper lifetime could be extrapolated from testing condition to normal working condition.

The second objective was to examine the failure mechanisms in solder bump electromigration which could be significantly different between various solder bump systems. Pb-free and high-Pb solder alloys with different UBM configurations were studied. The research results showed that the most active region during solder bump electromigration was the under bump metallization (UBM) layer and its interface with the solder due to the intermetallic compound formation and UBM dissolution. Therefore, the electromigration-induced damage occurred mostly in this region. The failure mechanisms were found to be highly dependent on the material system as well as the temperature.

The third objective was to determine the statistical lifetime of the flip chip solder bumps under electromigration. Lognormal distributions were used to fit the lifetime. The temperature and current dependence was assumed to follow Black's equation and the activation energies was calculated from that. The results showed that

the traditional Black's equation might not be applicable to solder bump electromigration due to the different failure mechanism at different temperatures. Special attention is needed to set up design rules for maximum operating current and temperature for a solder bump structure when extrapolating data from high temperature.

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Chapter 1: Introduction

The growth of the semiconductor industry has followed Moore's Law for the past 30 years. This means that the numbers of transistors on the integrated circuit doubles every 18 months. The growth has been sustained by scaling-down of features not only on the wafer but also at the package level. Meanwhile power consumption has risen to support the growing functionality which leads to higher current and power densities. The increasing stress and less robust structures pose new reliability risks to microelectronic packages. Electromigration-related damage in solder bumps is one of these emerging issues. Intensive studies on electromigration phenomena have been carried out on silicon level interconnect lines since the first electromigration-induced failure was observed in the late 1960s. The electromigration phenomena in solder bumps have been found to be quite different than that in silicon level interconnects. A brief review of the theory of electromigration will be given first. It will be followed by an introduction of the flip chip interconnect structure and process. After that, the difference between the electromigration in chip level and flip chip solder interconnects will be discussed. Finally, an overview of the experimental studies performed within the scope of this investigation will be shown.

1.1 ELECTROMIGRATION IN SI LEVEL INTERCONNECTS

Electromigration, or electrotransport, generally refers to a mass transport process in metal under the influence of electrical field [1.1]. The essential elements of electromigration are diffusion and a driving force. The drift velocity v_d of the metal ions in electromigration can then be described by the Nernst-Einstein relationship as

$$v_d = \mu F = \frac{D}{kT} F \tag{1.1}$$

where μ is the ion mobility, D is the diffusivity, k is Boltzmann's constant, T is the absolute temperature and F is the driving force. The ion mobility or diffusivity can be readily estimated using other types of diffusion processes, while the understanding of the driving force of electromigration is not always as apparent. In most of the early work, the driving force was naturally considered to be the reduction of electrical potential energy as the metal atoms moved in response to the electrical field as shown in Figure 1.1 [1.2].

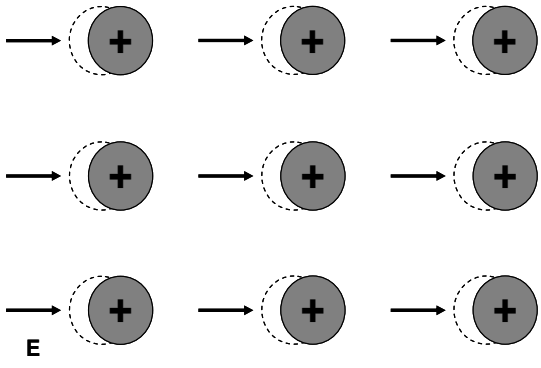
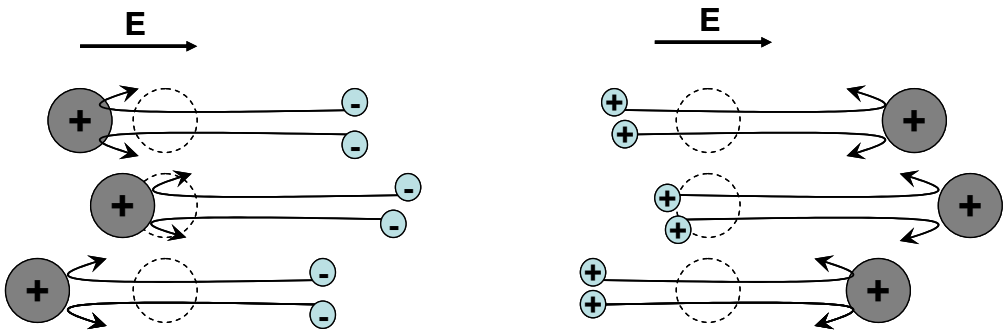


Figure 1.1 Movement of metal atom nuclei under pure static electric field

This hypothesis was challenged by the investigation by Seith and Wever in early 1950s [1.3, 1.4]. Their work showed that the direction of net mass (metal ions) transport in electromigration is the same as that of the prevailing charge carriers (electrons or holes) as illustrated in Figure 1.2, as if the ions are 'swept' by the electron (or holes) 'wind'. This suggests that the momentum exchange with moving charges might provide an important driving force for electromigration.



Electrons are the dominant charge carrier Holes are the dominant charge carrier

Figure 1.2 Movement of metal ions driven by the static electrical force and momentum exchange with charge carriers. The force generated by the momentum exchange prevails and the direction of net movement is then determined by the dominant carrier

Using a phenomenological approach, the effective driving force in electromigration can then be described as

$$F_{eff} = F_{el} + F_{wd} \tag{1.2}$$

where the effective driving force F_{eff} in electromigration is the sum of the electrostatic force F_{el} and the 'electron wind' force F_{wd}. The force exerted on a charged particle in an electrical field E is

$$F = qE = eZE \tag{1.3}$$

where e is the value of electron charge, Z is the charge number and E is the electrical field. Therefore, (1.2) can be re-written as

$$F_{eff} = eZ_{el}E + eZ_{wd}E = e(Z_{el} + Z_{wd})E = eZ^{*}E \tag{1.4}$$

Z_{el} is the valence of the ion and Z_{wd} is a virtual charge number that accounts for the electron wind force. The sum of the above two, Z*, known as the "effective charge number", is the parameter that measures the total strength of electromigration. Its value normally ranges from 10^{-1}~10^{2}.

By substituting (1.4) into (1.1), the drift velocity of the moving species can then be described as

$$v_d = \mu F_{eff} = \frac{D_{eff}}{kT} eZ^{*}E = \frac{D_{eff}}{kT} eZ^{*}\rho j \tag{1.5}$$

where ρ is the resistivity of the material and j is the applied current density. The atomic flux, J, in electromigration is the product of the drift velocity, v_d and the atomic density, n

$$J = nv_d = n\frac{D_{eff}}{kT} eZ^{*}\rho j \tag{1.6}$$

Equations (1.5) and (1.6) are frequently used in the analysis of electromigration because they demonstrate clear relationships between the micro-level mass transports (ν, J) and the macro-level driving force (E, j).

An important phenomena in interconnect line electromigration is the effect of stress-induced backflow discovered by Blech [1.5]. During electromigration, compressive and tensile stresses will build up in the regions where the atoms are swept into and out of by the electron wind force respectively. Consequently, stress gradients exist within the metal lines. These gradients result in a backflow of material ("Blech-effect").

$$J_{back} = nv_b = n\mu\Omega\frac{\Delta\sigma}{\Delta x} = n\frac{D}{kT}\Omega\frac{\Delta\sigma}{\Delta x} \tag{1.7}$$

where v_b is the average backflow velocity, Ω the atomic volume, and $\Delta\sigma$ is the stress difference between the compressive and tensile regions and $\Delta x \approx l$ is roughly the length of the interconnect line. Therefore, the total atomic flux under electromigration is,

$$J = J_{EM} + J_{\sigma} = C\frac{D}{kT}eZ^{*}\rho j - C\frac{D}{kT}\frac{\Delta\sigma\Omega}{l} \tag{1.8}$$

When J=0, a threshold value or a critical current density length product $(jl)_c$ is obtained below which net mass transport vanishes:

$$(jl)_c = \Omega\frac{\Delta\sigma}{Z^{*}e\rho} \tag{1.9}$$

In (1.9), Ω, Z* and ρ are fixed once the metallization material is chosen. However, design optimization can be done to minimize $\Delta\sigma$ through the selection of proper dielectric materials and structure layout so that the maximum $(jl)_c$ can be achieved.

1.2 FLIP CHIP TECHNOLOGY

1.2.1 Flip Chip Technology Overview

To keep up with the ever increasing I/O demand, the solder-bump flip-chip interconnection is increasingly used by the semiconductor industry. Flip-chip technology was developed in the early 1960s to improve the reliability and productivity as well as reduce cost of manual wirebonding. This type of interconnection is also called controlled-collapse-chip connection (C^4 or C4) which utilizes solder bumps deposited on wettable metal terminals on the chip and joined to a matching footprint of solder terminals on the substrate [1.6-1.8]. Because the entire chip area can be used for the bump array, the I/O density is greatly increased. Figure 1.3 is an illustration of a flip chip package. The upside-down chip (flip chip) is aligned to the substrate, and all connections are made simultaneously by reflowing the solder.

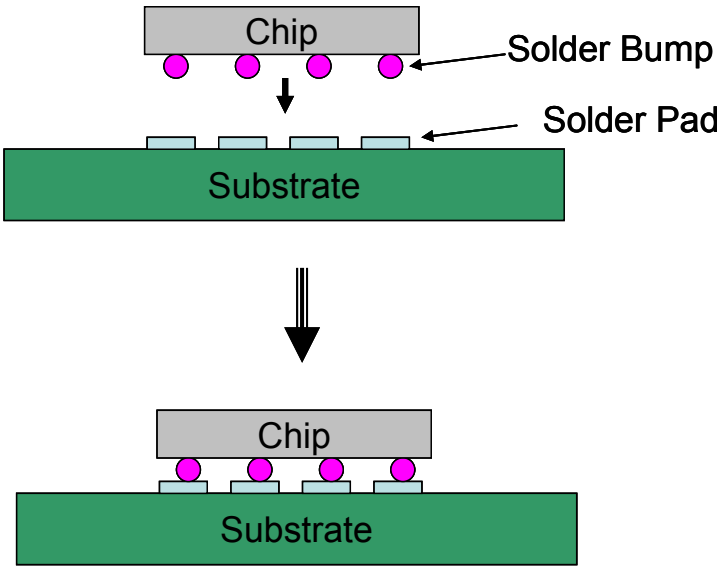


Figure 1.3 Illustration of Flip-chip package

Shown in Figure 1.4 is the schematic view of the cross-section of a reflowed solder bump. Because the solders usually do not wet the bare silicon or dielectric materials such as SiO_2, an under-bump metallization (UBM) layer is deposited on these substrates first in order to make the connection. The UBM usually consists of three layers:

(1) An adhesion layer, such as Cr or Ti, capable of forming a strong bond with the passivation such as SiO_2, and with the terminating Al pad.

(2) A solder wetting layer, such as Ni or Cu, which must remain at least partially intact throughout the assembly and test process. An additional requirement of the adhesion and/or wetting layer is to form a barrier system to preclude the penetration of solder into the chip wiring or under the passivation.

(3) A oxide-resistant layer, Au or other noble metal, to retain wettability for the solderable layer when vacuum is broken.

In the example in Figure 1.4, the adhesion layer is the Ti. A thin layer of Cu is then sputtered on top of the Ti layer to act as the electrode for electroplating of the next layer of Ni. The final Ni layer ensures good solder wettability with the solder alloy and act as a robust solder diffusion barrier to guarantee that the bump metals and bond pad metals do not react with each other to degrade the reliability of the system. There was an protective layer of Au which dissolved into the solder during the reflow process.

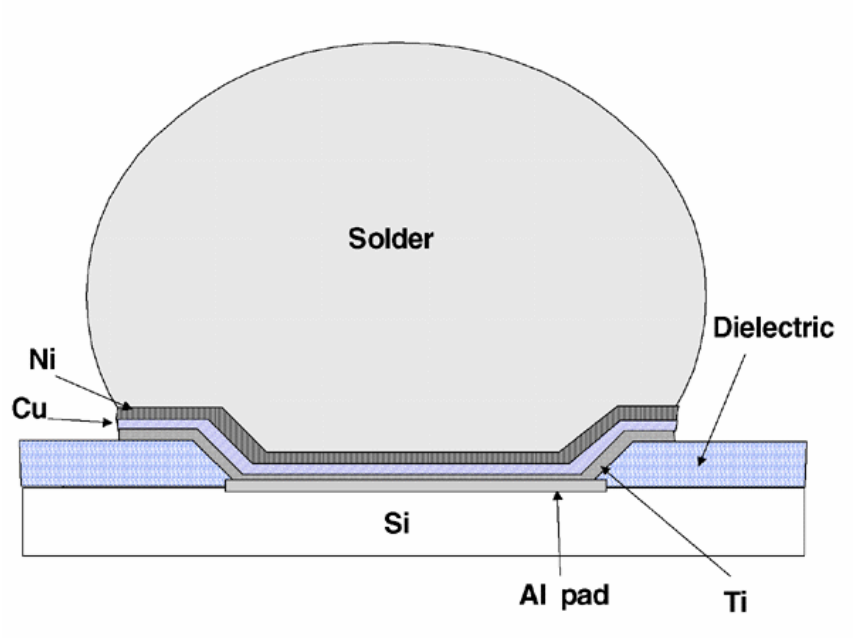


Figure 1.4 Typical structure of flip chip solder bumps [1.9]

The solder bump serves as the interconnection between the silicon chip and the rest of the electronic system. The solder self-centers and collapses when fully reflowed, making assembly less difficult and enhancing the reliability of the joint. The solder bump can take the shape of an hourglass, barrel, and drum depending on the distance between the chip and the substrate, pad size, and the volume of the solder. The two types of processes which are normally used to form the solder bump on silicon chip are the evaporative process and the electroplate process. These methods are shown in Figure 1.5 [1.6].

Solder bumps are deposited selectively in the evaporative process (Figure 1.5 (a)) through a molybdenum (Mo) shadow mask. The initial process step is to define the bump pad area with photolithography. This is followed by the evaporation of the under bump metallization. The next step is to evaporate the bump alloy to form the bulk of the bump. Finally, the bump is reflowed to homogenize the solder and allow the alloy to form an intermetallic compound with the UBM. This provides the necessary adhesion between the die and the bump.

The electroplate process begins with depositing the bump's UBM base structure on the wafer in blanket form using sputtering. A process that involves thick photo-resist coating, alignment, exposure, and development is used to define the remaining bump structures that are to be selectively electroplated on top of the sputtered UBM. The solder bump alloy of choice is plated to form the structure after the photo process. The photo-resist is stripped and the UBM layers are wet

etched away after plating is finished. Ashing, fluxing, reflowing, and cleaning complete the process (Figure 1.5 (b)).

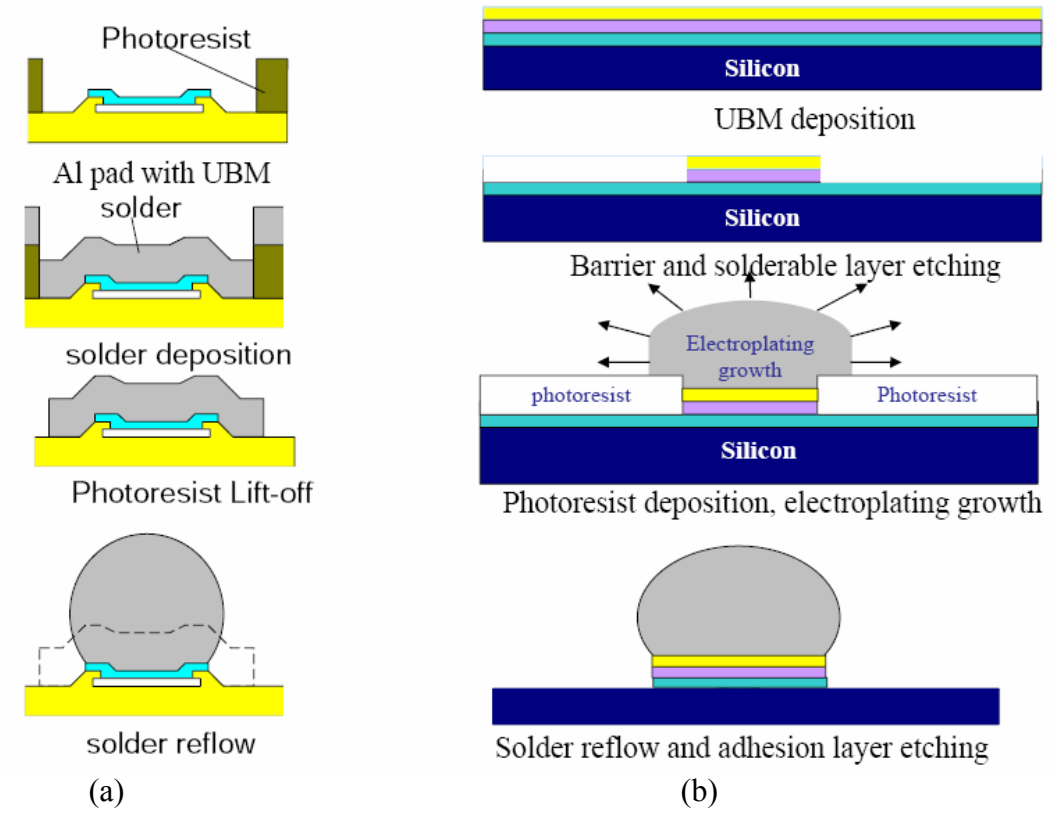


Figure 1.5 Two typical forming processes of flip chip solder bumps: (a) Evaporative; (b) Electroplated

1.2.2 Typical Solder Alloys Used for Flip Chip Bumps

Pb-Sn alloy has been used for soldering material for a long time. The first C4 bump was made with Pb-Sn alloy with over 90wt% Pb. It is still the most commonly used solder alloy in flip chip applications. The phase diagram of Pb-Sn

is shown in Figure 1.6 [1.30]. Typically two types of Pb-Sn systems are used. The high-Pb solder (95-97% by weight) has the melting temperature of 305-320^{o}C. It is normally jointed with ceramic substrates since the solder reflow process requires a peak temperature around 360^{o}C to ensure complete melting of the bump. The eutectic Pb-Sn alloy (37wt%Pb-63wt%Sn) has a melting point of 183^{o}C, and is used more often on organic substrates which can not survive temperature over 240^{o}C.

The employment of Pb-free alloys is greatly increased due to the environmental legislation for the past few years. Most of the Pb-free alloys so far are Sn-based with small amount of additive elements. One example is the Sn-Ag alloy. The phase diagram is shown in Figure 1.7 [1.30]. The eutectic Sn-Ag alloy (96.5wt%Sn-3.5wt%Ag) has a melting point of 221^{o}C, which is lower than the high-Pb alloy but higher than the eutectic Pb-Sn alloy. Data in the literature suggests that the thermo-mechanical reliability of Pb-free alloy can be as good as or better than eutectic Sn/Pb [1.10-1.16]. At the same time, new reliability issues may also arise with the introduction of Pb-free alloys. For example, due to Pb-free alloy's higher yield strength and lower ductility, electronic packages with Pb-free interconnect tend to have reduced mechanical robustness, a property critical for hand-held applications.

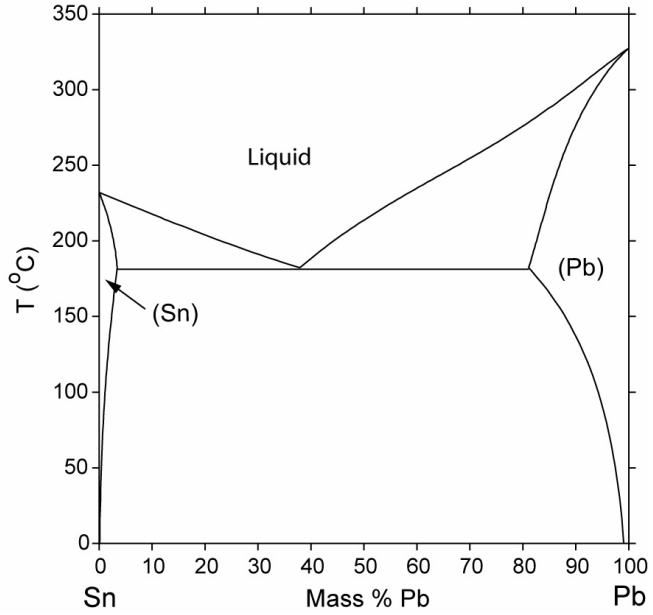


Figure 1.6 Sn-Pb phase diagram [1.30]

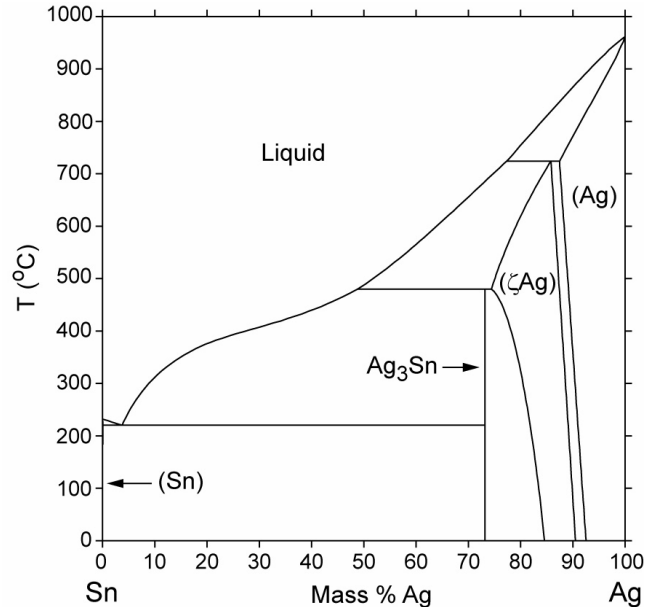


Figure 1.7 Sn-Ag phase diagram [1.30]

1.3 ELECTROMIGRATION IN SOLDER INTERCONNECTS

1.3.1 Overview

The growth of high-performance silicon devices requires a dramatic increase in the number of input/output (I/O) to meet the increasing number of signal lines and power requirements. This has driven the shrinkage of flip-chip interconnect pitch and size. The flip chip bump pitch has been reduced from 250 μm (1999) to 100μm (2006) and will continue to reduce to 50 μm by 2010 [1.17]. Current design rules have a maximum of ~100mA per bump. The maximum allowed current density will rise from ~$8x10^2$A/cm^2 to $2x10^4$A /cm^2 as bump pitch decreases. Current density will increase further as chip voltage decreases and maximum current level increases. A physical limit to increasing current density in both microelectronics and power electronics is electromigration. Electromigration of interconnect metal lines is the major failure phenomenon in integrated circuits (IC), but until recently it was seldom recognized as a reliability concern for solder bumps. Although research over the past four decades on Al(Cu) interconnect electromigration has developed effective models of the phenomena which have helped devise accelerated tests that reasonably predict long term reliability, extension of these models and accelerated tests to solder bumps has been made difficult by the differences between these two materials.

The interconnects on silicon dice are made of pure metal (Cu) or dilute alloys (0.5~4% Cu in Al). The primary driving force during the electromigration

is the 'electron wind' force. Since the normal operating temperature of interconnects (~100^{o}C) is less than 0.5T_m (melting temperature), the primary diffusion mechanism is the grain boundary diffusion [1.18, 1.19]. On the other hand, the solder interconnect is a much more complex material system with multiple elements and phases. For example, the solder interconnects depicted in Figure 1.4 not only have elements from the solder alloy which could be Pb and Sn, but also elements from the UBM such as Ti, Cu and Ni. The phases involved in the system are the solder alloy itself and the intermetallic compounds formed between the solder and UBM. Therefore, compositional gradient-induced chemical potential differences could play a role in electromigration, especially in the intermetallic compound phases where a large composition gradient exists. The influence of gradients on electromigration can be re-written as,

$$J = J_{EM} + J_{chem} + J_{\sigma} = C\frac{D}{kT}eZ^{*}\rho j + D\frac{\partial C}{\partial x} - C\frac{D}{kT}\frac{\partial \sigma \Omega}{\partial x} \tag{1.10}$$

With operation temperatures well above 0.5T_m, lattice diffusion in the solder is at comparable level to grain boundary diffusion. The physical properties of the Al, Cu and solder interconnect are summarized in Table 1.1.

Table 1.1 Comparison of Al, Cu and solder interconnect [1.31]

	Melting point T_m (^oC)	Operation Temperature (T/T_m)	Diffusion Species
Solder	138~310	0.64~0.91	Pb, Sn, Cu, Ni etc.
Al	660	0.4	Al
Cu	1083	0.28	Cu

1.3.2 Electromigration in Solder Lines

The study on the electromigration phenomena in solder alloys have been performed in line form. Huynh *et al.* prepared eutectic Sn-Pb solder lines with etched *V* grooves on (001) Si surfaces as shown in Figure 1.8 [1.20]. Electromigration tests were done in these lines at a current density of 2.8 $x10^4 A/cm^2$ at 150°C. As shown in Figure 1.9, a large lump of solder containing both Pb and Sn was observed to accumulate at the anode. The accumulated material is rich in Pb, suggesting that Pb diffuses faster than Sn at this temperature. Accordingly, voids were found at the cathode (Figure 1.9). Similar results were found in Sn solder lines with small additions (0~3%) of Cu at current densities of $2x10^4 A/cm^2$ and 150^oC ambient [1.21].

We note that the current density required for electromigration failure to occur in solder lines is about two orders of magnitude less than that necessary for interconnect lines ($\sim 10^6 A/cm^2$). This could be due to the much smaller backstress and critical jL_c in the solder lines [1.22]. Recall Eq.(1.9), jL_c is determined by the

atomic volume, Ω, the electric resistivity, ρ, the effective charge number, Z^* and the stress difference between anode and cathode, $\Delta\sigma$. The Ω, ρ and Z^* from various sources [1.32-1.35] are summarized in Table 1.2.

Table 1.2 Parameters that determine the jL_c

	Ω (cm^3)	ρ (10^{-6}Ω.cm)	Z*
Solder	~$3x10^{-23}$	10~20	-33 ~-39
Al or Cu	~$2x10^{-23}$	2~3	-6.4~-4.8

From Table 1.2 one can see that the resistivity and effective charge number of solder alloy are about one order of magnitude larger than those of the Al or Cu interconnects. The stress difference built up in the solder lines can be estimated by replacing $\Delta\sigma$ by $Y\Delta\varepsilon$, where Y is Young's modulus and $\Delta\varepsilon$ = 0.2 % is the elastic limit. The Young's modulus of eutectic Sn-Pb (30 GPa) is a factor of two to four smaller than those of Al (69 GPa) and Cu (110 GPa). Therefore, if one keeps l in (1.7) as a constant for comparison, the critical current density necessary to cause electromigration damage in solder is about two orders of magnitude smaller than that needed to cause electromigration in Al and Cu interconnects. The jL_c will be smaller if the creep and stress relaxation processes are considered.

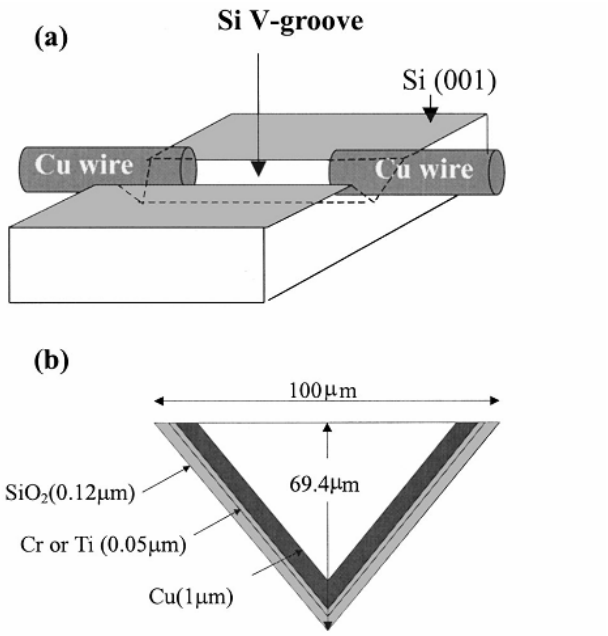


Figure 1.8 Schematic diagram of (a) V-groove on (001) Si surface with two Cu wires as electrodes at the two ends and (b) the cross-section of a V groove and its dimensions [1.20]

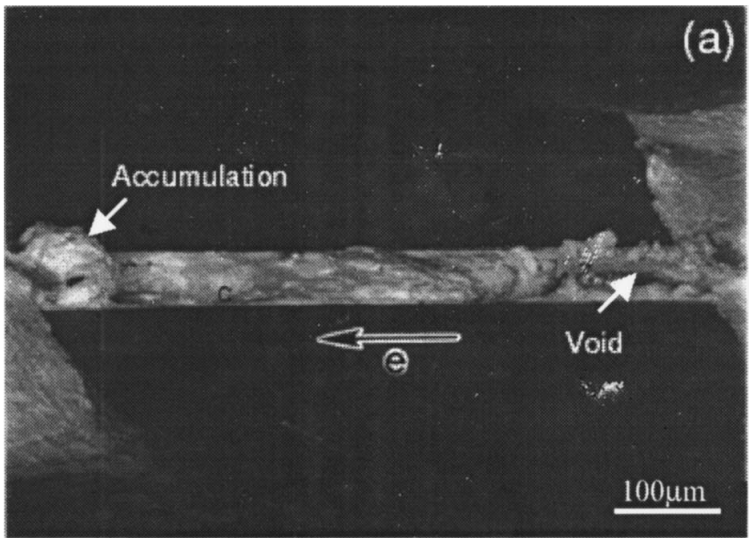


Figure 1.9 SEM images of a eutectic Sn-Pb solder line of 800 μm width and 150μm length stressed by $2.8 \times 10^4 A/cm^2$ 150°C in ambient [1.20]

1.3.3 Electromigration in Flip Chip Solder Bumps

Electromigration studies of flip chip solder bumps have shown that the failure mechanism of the flip chip solder joint system can be appreciably different than that of the solder lines [1.23-1.26]. Most of the work did not find noticeable piling up of the solder alloy at the anode side of the joint. Instead, significant microstructure changes within the solder joint were observed including phase separation, intermetallic compound growth, and the dissolution of the under bump metallurgy. For example, Lin *et al.* reported enhanced phase segregation during electromigration tests of the eutectic Pb-Sn solder bumps [1.27]. As shown in Figure 1.10, without current stress, Pb and Sn rich phases were uniformly distributed inside the bump. When current stress was applied, the Pb and Sn rich phases were separated from each other with Pb-rich phase moving faster along the electron current direction.

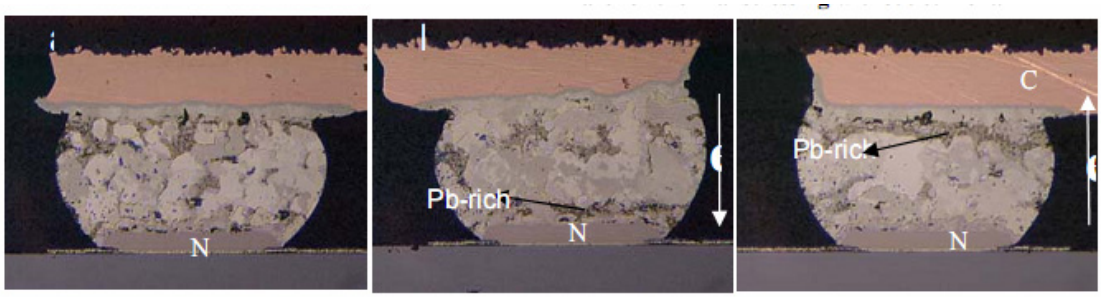


Figure 1.10 Cross-section of Sn-Pb bumps after 150^{o}C stress for 2338 hrs: Left: no current, middle: 0.5A with electron flowing from top to bottom, and right: 0.5A with electron flowing from bottom to top [1.27]

The enhanced consumption of under bump metallization is another common observation from the literature. Hu *et al.* reported electromigration

failure in solder bumps included a very rapid dissolution of the Cu metallization on the cathode side (Figure 1.11) [1.28]. The average dissolution rate was about 1 μm/min. The dissolved Cu included not only the Cu under bump metallurgy but also the on-chip Cu conducting trace.

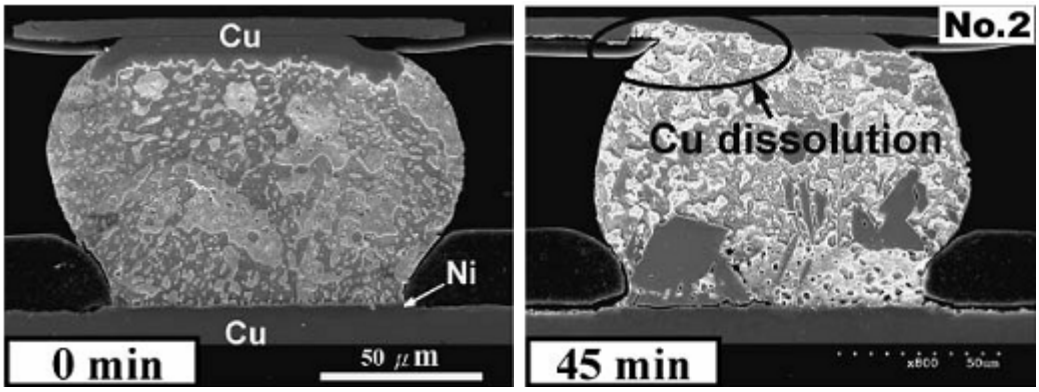


Figure 1.11 Fast dissolution of Cu trace in solder bumps during EM test [1.28]

The fast dissolution of the UBM layers is not unexpected since the materials used for the UBM are transitional metals and they have been known to have fast diffusion in Pb and Sn as discussed by Warburton *et al.* [1.29]. The diffusivity of two common UBM elements, Cu and Ni, in Pb and Sn in the solder electromigration testing temperature range are listed in Figure 1.12. One can see that the diffusivity of Cu and Ni is several orders of magnitude higher than that of the Pb and Sn themselves. The diffusion flux of the UBM atoms will be enhanced even more due to the fact that the UBM layers are closer to the current crowding

region (will be discussed in Chapter 4) and subjected to a larger current densities than the main body of the solder bump.

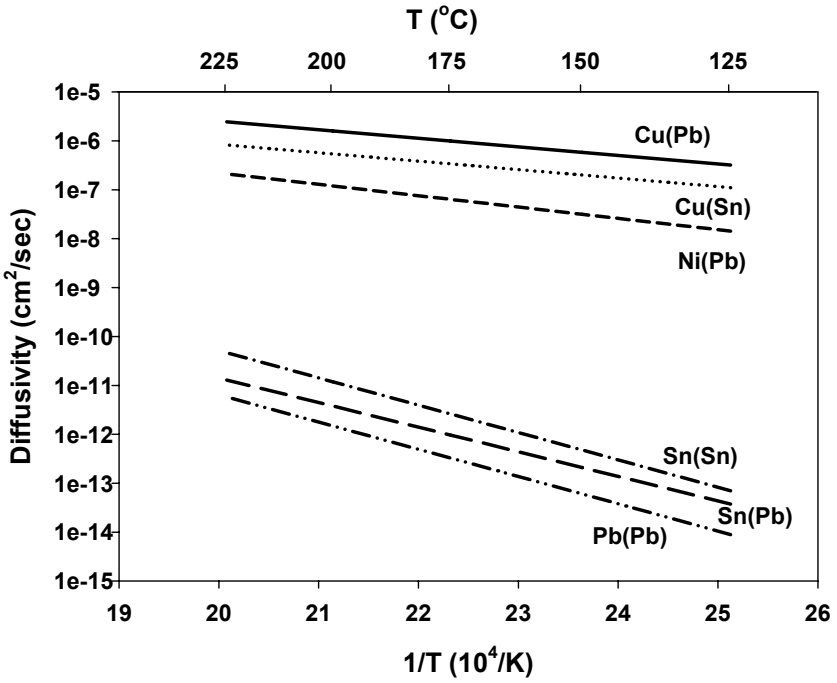


Figure 1.12 Diffusivity of various elements in Pb and Sn [1.29]

1.4 OBJECTIVES AND APPROACH

There are three objectives of this study. The first objective is to set up an effective experimental technique to examine the damage development and determine the failure time in the electromigration tests. The structure and dimensions of the flip chip solder bump is considerably different than that of chip level interconnects. Therefore, the traditional failure tracking method based on 2-

point resistance monitoring is no longer able to provide real-time damage evolution information. A test system based on a Wheatstone bridge circuit capable of detecting milli-ohm resistance change will be introduced in Chapter 3. More experimental details such as measurements of test structure temperature and statistical analysis will be discussed. The effectiveness of the test methodology will be examined for actual applications in Chapter 4 and 5.

The second objective is to identify the failure mechanisms in solder bump electromigration which depend on the solder bump systems. As briefly mentioned in the previous section, the most active region during the solder bump electromigration is at the UBM layer and its interface with the solder as a result of the UBM dissolution and intermetallic compound formation. Therefore, the theory of intermetallic compound formation under the influence of current will be introduced in Chapter 2. In Chapter 4 and 5, studies will be carried out in flip chip products with Pb-free and Sn-Pb solder alloys with different UBM configurations. The failure mechanisms will be compared and explained based on the analysis of the IMC growth.

The third objective is to determine the statistical lifetime of the flip chip solder bumps under electromigration. This is the ultimate goal of this study so that design rules can be set up for maximum operating current and temperature under certain reliability requirements. Lognormal distributions will be used to fit the lifetime data in Chapter 4 and 5. The temperature and current dependence will be assumed to follow Black's equation and the activation energies will be measured

from that. The correlation between the lifetime and the failure mechanism will be discussed.

Chapter 7 summarizes the study and gives some suggestions for future studies.

Chapter 2: Intermetallic Compound Growth in Solder Joint

The intermetallic compound formed between the solder bump and the solder pad metallization serves as the interfacial adhesion layer. Therefore, the formation, growth and dissolution of the intermetallic compounds will affect the integrity of the solder joint. In this chapter, a brief review of the intermetallic compounds that can be found in the flip chip solder bumps will be reviewed first. It will be followed by the analysis of the solid state growth of intermetallic compound with and without current stressing to demonstrate the impact of electromigration. Finally, a two dimensional model will be introduced to describe the kinetics of the damage evolution near the intermetallic compound/solder interface.

2.1 INTERMETALLIC COMPOUND IN SOLDER JOINT

Sn is the major active element in both Sn-Pb and Pb-free solder bumps that reacts with the UBM metal layer to form intermetallic compounds. The most common elements in the UBM structures are Cu and Ni layers deposited by physical evaporation deposition (PVD), electro-chemical and electroless plating. The Cu-Sn, Ni-Sn and Cu-Ni-Sn intermetallic compounds are commonly seen in the flip chip solder bumps.

The Cu–Sn system is characterized by a series of peritectic reactions and the corresponding intermetallic phases, as shown in Figure 2.1 [2.1]. The

temperature of the semiconductor package soldering process is usually lower than 350°C. The interfacial reaction between Cu and Sn-based solder results in the formation of Cu_6Sn_5(η) and Cu_3Sn(ε) phases in this temperature range [2.2-2.5]. During the soldering process, Cu_6Sn_5 is the first phase to appear at the interface. It has two forms, η and η'. η' is the stable form which transforms into η at a temperature around 186°C. The subsequent reaction between Cu and Cu_6Sn_5 forms Cu_3Sn. Observations by transmission electron microscopy (TEM) show that ε-phase does not form at temperatures below 60°C. At temperatures above 60°C, the ε-phase grows together with the η'-phase [2.6-2.8].

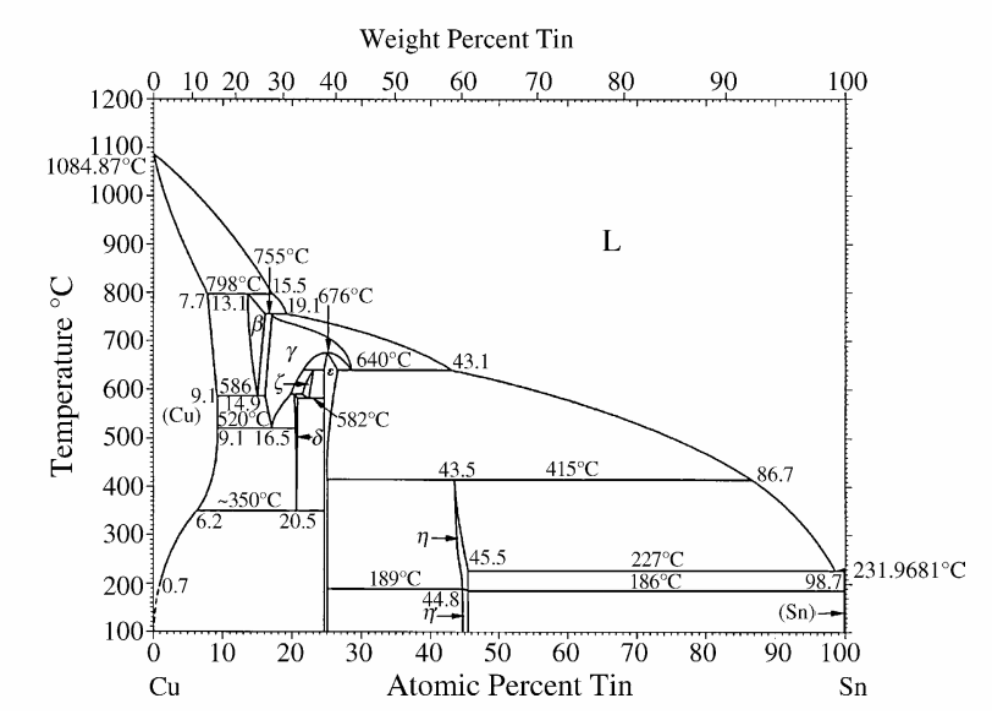


Figure 2.1 Cu-Sn Phase diagram [2.1]

With the growth of the intermetallic, Kirkendall voiding will appear in at the Cu/Cu_3Sn interface and inside Cu_3Sn layers as can be seen in Figure 2.2[2.9]. It has been reported that the formation of Kirkendall voids during solid state annealing is dependent on the quality of Cu. Cu layers with high impurity levels, such as the electrochemically deposited Cu, is more likely to have Kirkendall voids grown than high purity oxygen-free high conductivity (OFHC) Cu layers.

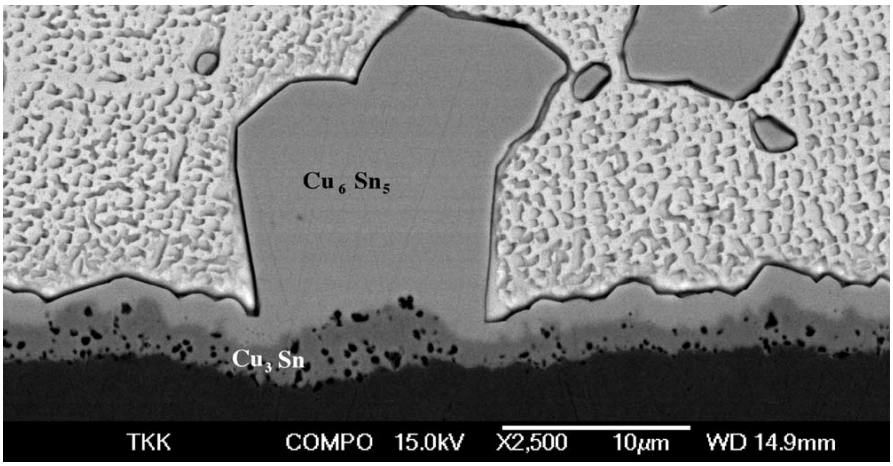


Figure 2.2 Kirkendall voiding in the intermetallic layers in Cu/Sn diffusion couple annealed at 125°C for 1000 hours [2.9]

The phase diagram of Ni-Sn system is shown in Figure 2.3 [2.1]. Three intermetallic phases exist in the temperature range of interest, Ni_3Sn, Ni_3Sn_2 and Ni_3Sn_4. The Ni_3Sn_4 phase is found to be the first phase to form during the soldering process. The thickness of the Ni_3Sn_4 layer formed during soldering process is much smaller compared with the Cu-Sn system due to the low solubility of Ni in molten Sn and the slow reaction rate between Ni and Sn.

During solid-state annealing, the growth of the Ni_3Sn_4 layer was found to be significantly lower than that of Cu_6Sn_5 as can be seen in Figure 2.4 [2.10]. Overall, the consumption rate of Ni is much lower than Cu when joined to both Sn-Pb and Pb-free solders.

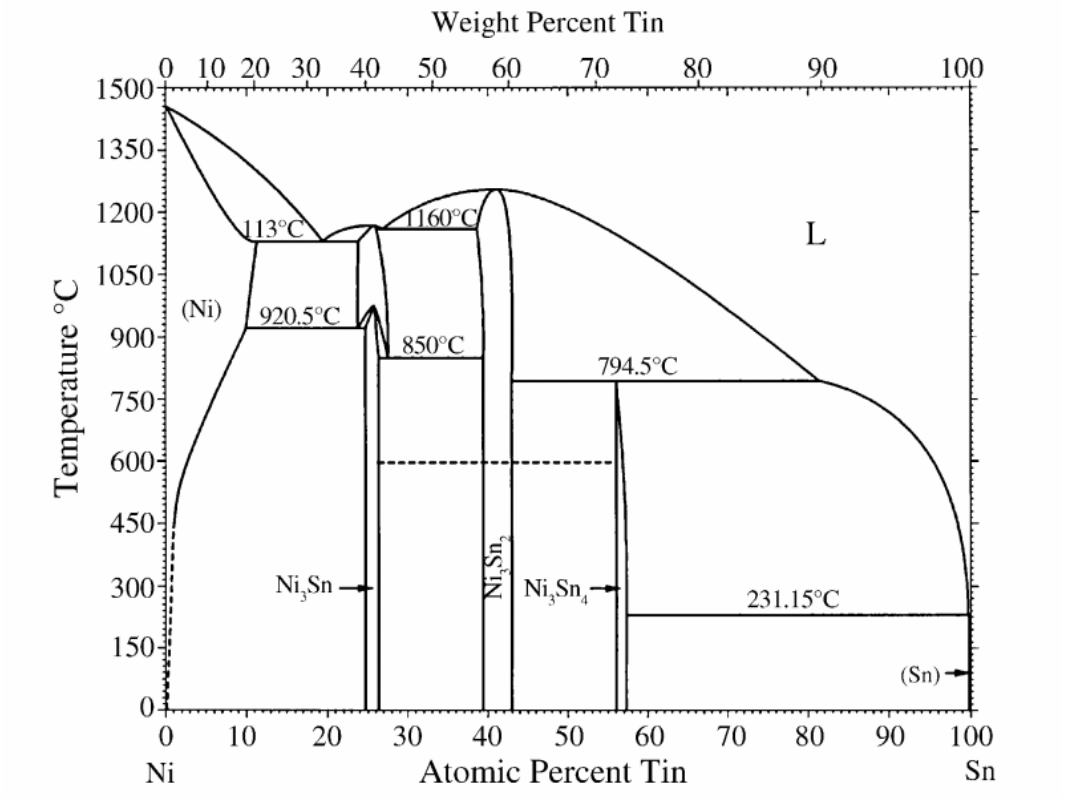


Figure 2.3 Ni-Sn Phase diagram [2.1]

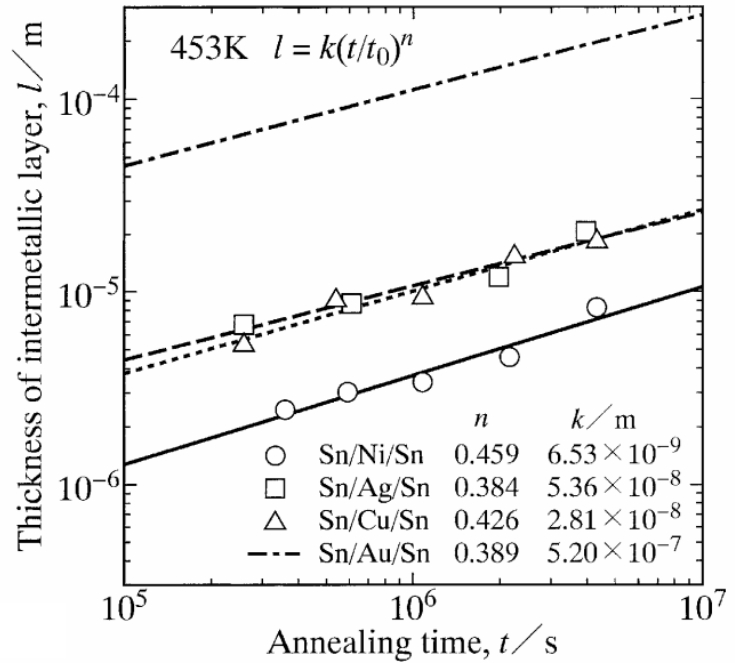


Figure 2.4 Thickness change with time during solid-state annealing at 453K of different diffusion couples [2.10]

In the alloys system with Cu, Ni and Sn, $(Ni,Cu)_3Sn_4$ and $(Cu,Ni)_6Sn_5$ phases, which are essentially Ni_3Sn_4 and Cu_6Sn_5 with of Cu and Ni dissolved, will form depending on the concentration of the alloy [2.11-2.13]. The addition of Ni stabilizes Cu_6Sn_5 considerably with much reduced Gibbs free energy.

2.2 GROWTH OF THE INTERMETALLIC COMPOUND

The growth of the intermetallic compound occurs at the phase boundaries through the interdiffusion of different atom species. A schematic drawing of the interfacial region of two metal phases (α and γ) with one intermetallic layer (β) is

shown in Figure 2.5. It is assumed that the diffusion of A atom into the B-rich phase is much faster than that of B atom into A (such as the case of Cu-Sn diffusion couple mentioned in chapter 1). Therefore, the growth of the intermetallic layer is induced by the A atoms diffusing through the intermetallic layer β and reaching the interface between β and γ. If no electrical current is applied, the diffusion is driven mainly by the concentration difference of A between the two boundaries of β. According to Fick's 1st law, the atomic flux, J_{diff}, of A is then

$$J_{diff} = -D\frac{\partial C}{\partial x} \approx -D\frac{\Delta C}{x} = -D\frac{(C_{\beta\gamma} - C_{\alpha\beta})}{x} \tag{2.1}$$

where D is the diffusivity of A in β, x is the thickness of β, $C_{\alpha\beta}$ and $C_{\beta\gamma}$ are the concentration of A at phase boundaries respectively. The growth rate of the intermetallic layer is then

$$\frac{dx}{dt} = \frac{J_{diff}}{(C_\beta - C_\gamma)} = -\frac{D}{(C_\beta - C_\gamma)}\frac{\Delta C}{x} \tag{2.2}$$

where C_β and C_γ are the atomic densities of A in β and γ respectively. Rearranging the equation and integrating both sides, one gets the correlation between the thickness of the intermetallic layer and time,

$$\int x dx = \int -\frac{D\Delta C}{(C_\beta - C_\gamma)} dt \Rightarrow x^2 = At + C \tag{2.3}$$

where $A=-2D^*\Delta C/\rho$ and C is the integration constant. Assuming that the thickness of the intermetallic compound is zero and time zero, C equals to zero. Therefore,

$$x \propto \sqrt{t} \tag{2.4}$$

which implies that the growth of the intermetallic compound will follow a square root correlation with respect to time.

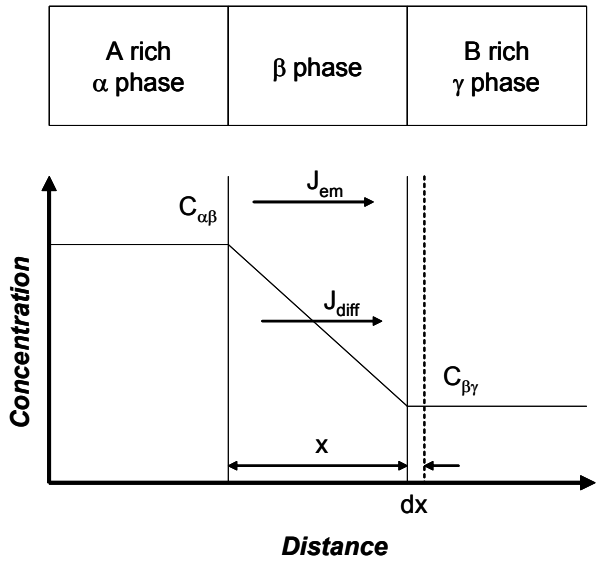


Figure 2.5 At the interface between α and γ phases, the intermetallic compound phase β forms a planar layer

When electron current is applied, additional atomic flux, J_{em}, is added due to electromigration. Assuming that there are more than one element in the material system, the flux for the *i*th element driven by electron current can be expressed as,

$$J_i^{EM} = C_i \frac{D_i}{kT} Z_i^* e \rho_i j \tag{2.5}$$

Two or more compounds will form simultaneously at the phase boundaries in many binary alloy couples,. The growth rate can not be expressed in analytical form in these cases. In stead, numerical simulation is needed. Chao *et al.* studied the IMC growth under electron current stressing in Cu-Sn system with the finite difference method [2.14]. According to phase diagram, both Cu_3Sn (ε) and Cu_6Sn_5 (η) will form between the Cu and Sn phases. Figure 2.6 shows the schematic composition profile of the diffusion couple.

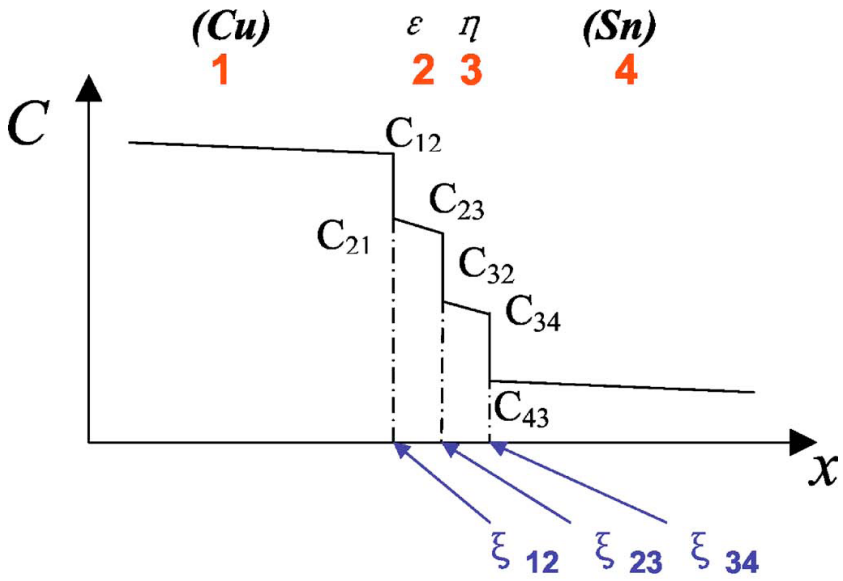


Figure 2.6 Cu composition profile of Cu–Sn diffusion couple [2.14]

The atomic flux due to chemical diffusion can be expressed as

$$\begin{aligned} J_{Cu,i}^{Chem} &= -D_{Cu,i}\frac{\partial C_{Cu,i}}{\partial x} = -D_{Cu,i}\frac{\partial C_i}{\partial x}, \\ J_{Sn,i}^{Chem} &= -D_{Sn,i}\frac{\partial C_{Sn,i}}{\partial x} = D_{Sn,i}\frac{\partial C_i}{\partial x} \end{aligned} \tag{2.6}$$

where all compositions C_i are expressed as mole fractions of Cu. The running index i denotes the phase in which interdiffusion takes place. It is assumed that the vacancy concentration is low, therefore the density of the phase is C_0=C_{Cu}+C_{Sn}. The current-induced atomic flux can be expressed as

$$\begin{aligned} J_{Cu,i}^{EM} &= C_i\frac{D_{Cu,i}}{kT}Z_{Cu,i}^{*}e\rho_i j, \\ J_{Sn,i}^{EM} &= (C_0 - C_i)\frac{D_{Sn,i}}{kT}Z_{Sn,i}^{*}e\rho_i j \end{aligned} \tag{2.7}$$

Combining the chemical diffusion flux and current-induced flux into Fick's second law gives the governing equations of current enhanced interdiffusion within each phase.

$$\begin{aligned} \frac{\partial C_i}{\partial t} &= \frac{\partial}{\partial x}\left[D\frac{\partial C_i}{\partial x} + \phi_i C_i(1-C_i)j\right], \\ \phi_i &= \frac{D_{Sn,i}}{kT}Z_{Sn,i}^{*}e\rho_i j - \frac{D_{Cu,i}}{kT}Z_{Cu,i}^{*}e\rho_i j \end{aligned} \tag{2.8}$$

Eq. (2.8) can be solved by using a finite difference method to give the moving speed of the phase boundaries and the growth rate of each intermetallic phase. Detailed deduction can be found in [2.14] and [2.15]. The numerical

solution of Cu-Sn diffusion couple with and without current stressing is shown in Figure 2.7 and 2.8. The temperature applied was 150^{o}C and the current density was 4X10^{4}A/cm^{2}. Figures 2.7(a) and (b) show the initial and final composition profiles of the solder joint after 300h with current stressing. It can be seen that both Cu_3Sn and Cu_6Sn_5 thickened at the expense of the Cu UBM. Cu_3Sn thickened but remained a thinner layer between Cu UBM and Cu_6Sn_5, whereas Cu_6Sn_5 grew far into the pure Sn solder.

The simulated thickness change over time of Cu_3Sn and Cu_6Sn_5 are plotted Figure 2.8(a) and (b). The thickness of Cu_6Sn_5 is greatly enhanced by current stressing and follows linear relationship with respect to the time. The growth of Cu_3Sn is impaired by the current although the magnitude between stressing and no stressing is small.

In Figure 2.7(c), an interesting result from this analysis is that a high concentration of vacancies can exist trailing the advancing Cu/Cu_3Sn interface under EM. Given the high concentration of vacancy at this region, Kirkendall voids are likely to form as a result of excess of vacancies. The predicted high vacancy concentration and subsequent void formation are consistent with experimental observations. Under EM tests at the nominal temperature of 150 °C, the dominant failure mode of the solder bumps tested was due to void formation at the Cu_6Sn_5 side of the Cu_6Sn_5/Cu_3Sn interface as can be seen in Figure 2.7(d).

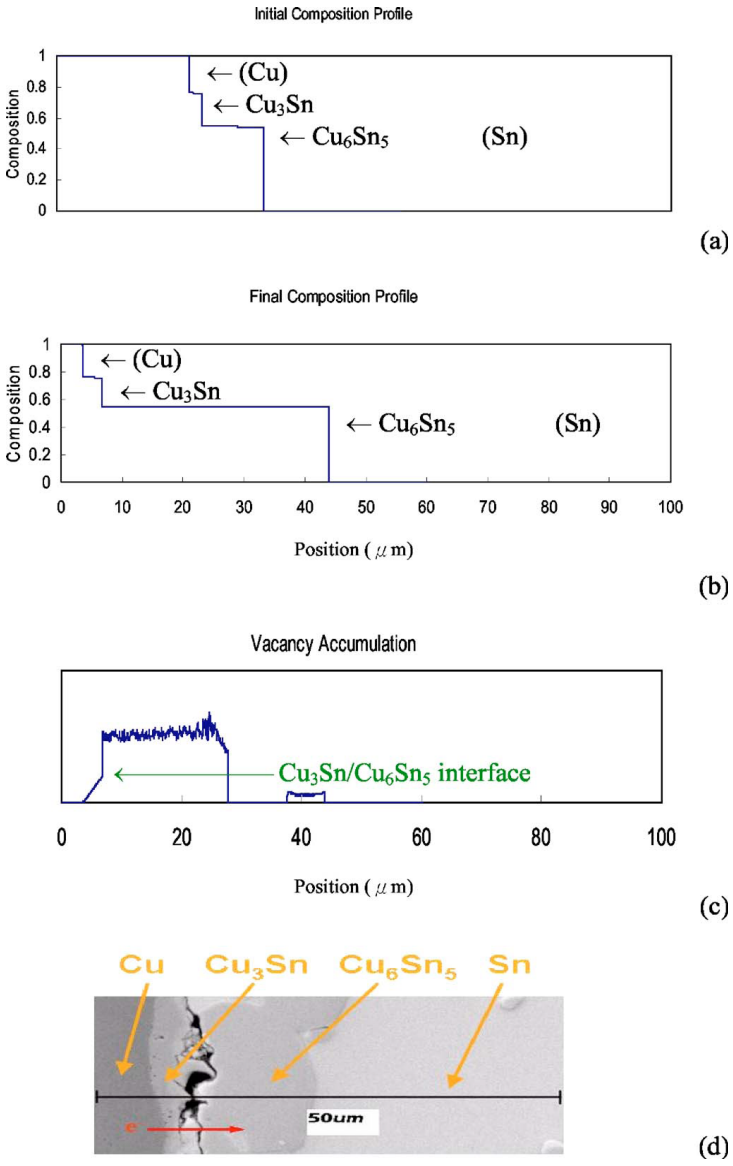


Figure 2.7 (a) Initial composition profile of simulation (0 hr); (b) Final composition profile of simulation (300 hr); (c) Vacancy accumulation derived from vacancy transport model; (d) Expanded SEM image of a failing solder joint showing the interfaces of intermetallic phases [2.14]

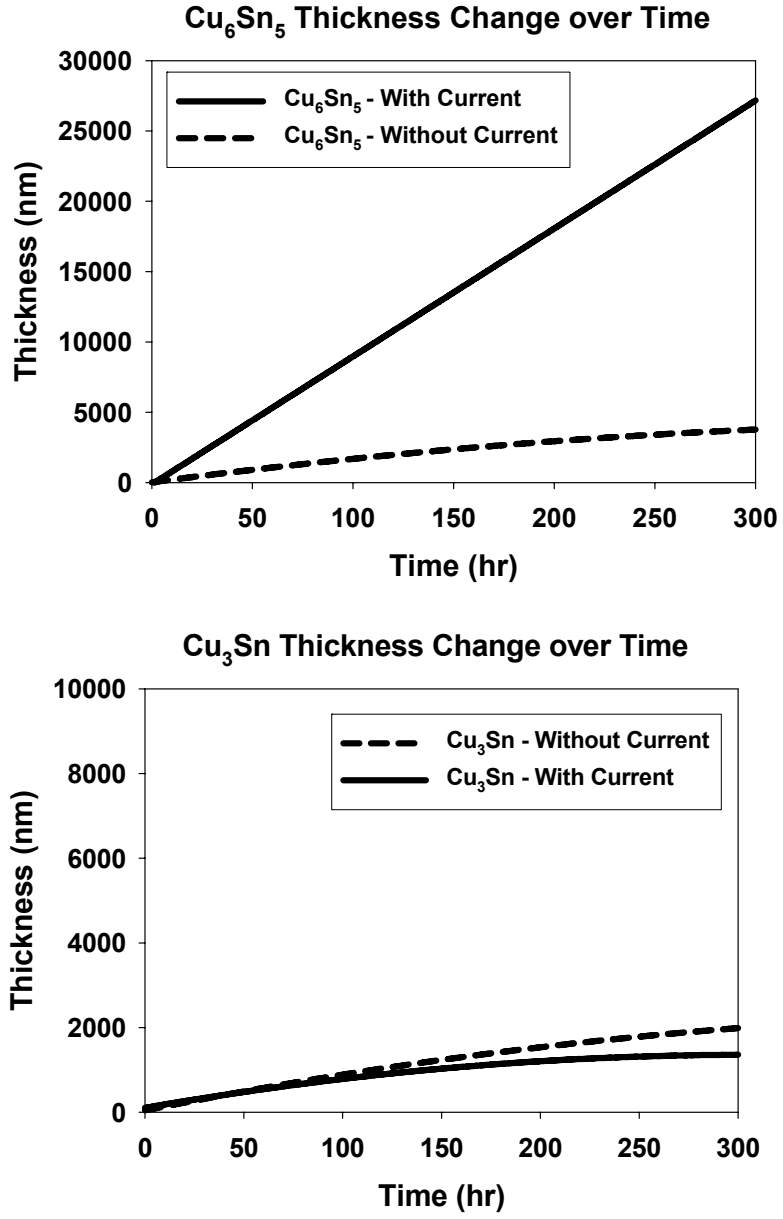


Figure 2.8 IMC thickness change plotted as a function of time (a) Cu_3Sn and (b) Cu_6Sn_5. (re-plotted from [2.14])

2.3 KINETICS OF THE ELECTROMIGRATION DAMAGE EVOLUTION

The studies discussed in previous sections provide the basic understanding on the microstructure evolution near the UBM-solder interface during electromigration. However, the electromigration lifetime can not be deducted directly by studying the intermetallic compound growth since the growth of the intermetallic itself does not lead to physical failures. Instead, the analysis of the damage evolution is necessary.

Zhang *et al* gave such an example using a 2-D model [2.16]. The analysis was performed to describe the propagation of a pancake-shape void along the UBM-solder interface under the influence of electron current, as shown in Figure 2.9. Voids propagating along the contact interface of UBM (or the intermetallic) and solder has been frequently observed in solder EM studies [2.17]. The schematic drawing of the 2-D model in Zhang's work is shown in Figure 2-10. During the electromigration test, as the atoms in the intermetallic compound and solder are being swept away from the interfacial region by the electron current, vacancy fluxes flow in the opposite direction toward the interface. Due to current crowding effect, most of the fluxes are concentrated in a narrow region, *b'*. The vacancy flux flowing into the intermetallic compound, J^v_{IMC}, is small compared with that in the solder, J^v_{solder}, since the bonding in the intermetallic compound is stronger and the vacancy formation energy is larger. Therefore, a flux divergence of vacancy occurs at the interface. The saturation of vacancies at the interface will lead to void nucleation and

condensation. The void will grow since it serves as a sink to absorb vacancies supplied by electromigration.

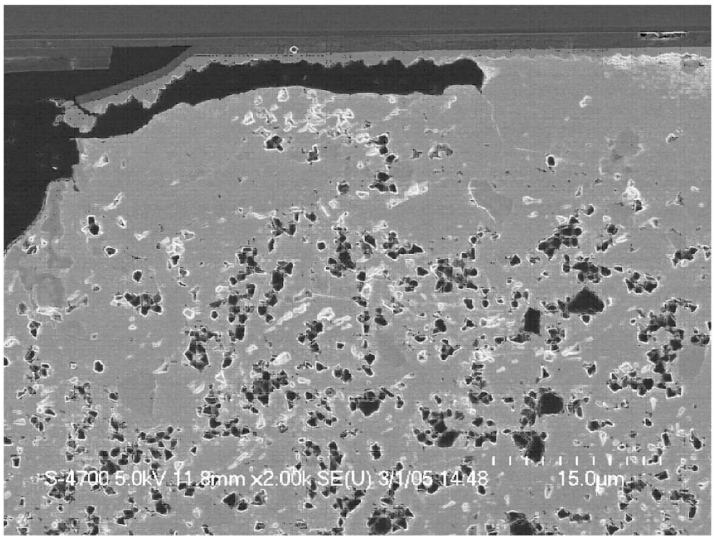


Figure 2.9 Pancake-shape crack growth at the UBM/solder interface [2.16]

The growth of the void can be calculated by analyzing the atomic fluxes at the intermetallic compound/solder interface. In a unit time, Δt, the void volume growth, ΔV, is

$$\Delta V = v\Delta td \tag{2.9}$$

where v is the speed of the pancake void front, d is the diameter of the front assuming a half-circle shape. The growth is sustained by the vacancy flow in the interfacial area within a width δ,

$$\Delta V = J^{v}_{\text{int}} \delta \Delta t \Omega \tag{2.10}$$

where Ω is the atomic volume. The interfacial flux is the difference between the vacancy flow in the solder and the intermetallic compound. Considering mass conservation, one gets,

$$J^{v}_{\text{int}} \delta = (J^{v}_{solder} - J^{v}_{IMC}) b' \tag{2.11}$$

Combining (2.9)-(2.11), the void front growth speed can be expressed as,

$$v = (J^{v}_{solder} - J^{v}_{IMC}) \frac{b'\Omega}{d} \tag{2.12}$$

where J^{v}_{solder} and J^{v}_{IMC} are the vacancy fluxes induced by electromigration,

$$J^{v}_{IMC} = \frac{C^{Bulk}_{IMC} D_{IMC}}{kT} Z^{*}_{IMC} e \rho_{IMC} j \tag{2.13}$$

$$J^{v}_{solder} = \frac{C^{Bulk}_{solder} D_{solder}}{kT} Z^{*}_{solder} e \rho_{solder} j \tag{2.14}$$

where j is the current density, Z^{*} is the effective charge number, D is the diffusivity. Because $C^{Bulk}\Omega=1$,

$$v = \frac{ej}{kT} (D_{solder} Z^{*}_{solder} \rho_{solder} - D_{IMC} Z^{*}_{IMC} \rho_{IMC}) \frac{b'}{d} \tag{2.15}$$

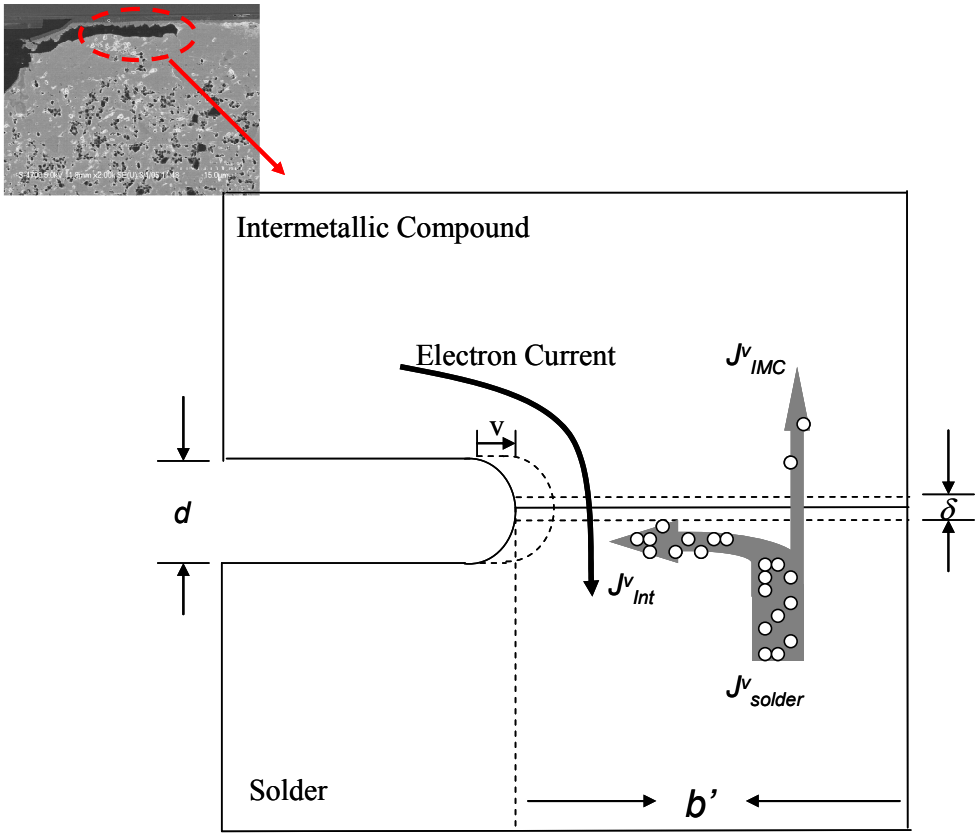


Figure 2.10 Schematic drawing of the IMC-solder interface during electromigration test

The growth rate of the void can be estimated using (2.15). For example, in the Cu/Sn diffusion couple, the diffusivity D_{solder} and D_{IMC} are $2.4\text{x}10^{-8}\text{cm}^2/\text{s}$ and $5.6\text{x}10^{-12}\text{cm}^2/\text{s}$ respectively [2.14]. Z^*_{solder} and Z^*_{IMC} are 2 and 33 [2.14]. ρ_{solder} and ρ_{IMC} are $13\text{x}10^{-6}\text{cm}\cdot\Omega$ and $18\text{x}10^{-6}\text{cm}\cdot\Omega$ [2.18]. b' and d is ~30μm and ~3μm. Therefore, at 150^{o}C with a current density of $10^4\text{A}/\text{cm}^2$, the growth rate of the

void is estimated to be ~0.017μm/s. According to Eq. (2.15) the growth rate changes linearly with the current density.

Chapter 3: Experimental Techniques

3.1 OVERVIEW

The electromigration phenomena of the die level interconnect lines are normally examined by monitoring the resistance change of the lines induced by the EM damage while a constant current is passed through them. Similar metrology is applied to solder EM studies, although certain changes have to be made to ensure useful results. First of all, the test current required for solder EM study (~1A) is about three orders of magnitude higher than that for interconnects due to the larger geometrical dimensions. A larger current will not only demand a current source with a higher capacity but also generates a serious Joule heating problem in the test structures. Secondly, because the resistance of the solder joint (several milli-ohms) is about 3 orders of magnitude smaller than that of the interconnects, a high sensitivity test circuitry is necessary to track the small changes in resistance during the EM test. In this chapter, experimental techniques to address these issues are described.

3.2 HIGH PRECISION CURRENT SOURCE

To obtain sufficiently large (>1 A) and stable (<0.1% variation) current needed for a solder joint EM test, a high precision, constant-current circuitry is used, as shown in Figure 3.1. The test current passing through the test structure, I_{test}, is determined by

$$I_{test} = \frac{V_{in}}{R_{sense}} \tag{3.1}$$

A high precision, low temperature coefficient voltage source (National Semiconductor LM136-5.0) and resistor were used to obtain stable V_{in} and R_{sense}. At the same time, an operational amplifier and a metal-oxide-semiconductor field-effect transistor (MOSFET) were used to form a feedback loop to regulate the current.

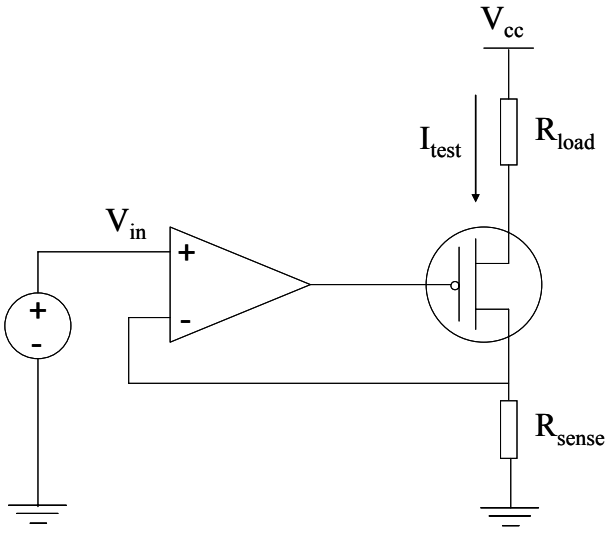


Figure 3.1 Schematic drawing of the constant-current circuitry

System calibration was carried out to check the current stability. As shown in Figure 3.2, constant current with fluctuations less than 0.5 milliamps over 1800 hours was achieved.

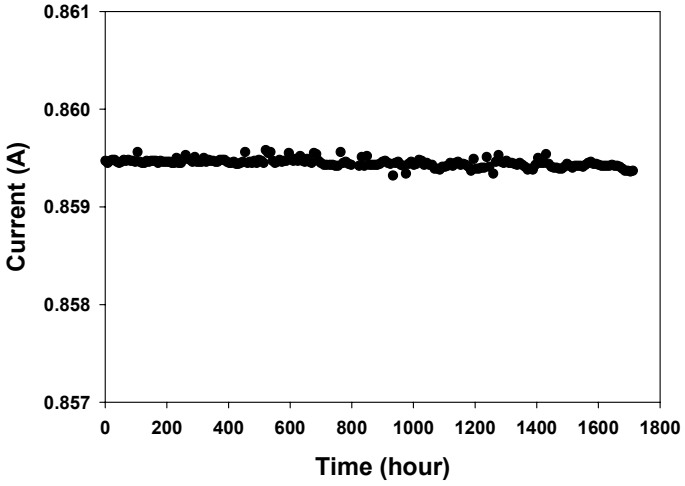


Figure 3.2 Performance of the constant-current source

3.3 WHEATSTONE BRIDGE METHOD

Due to the large cross-sectional area and the short length, the resistance of solder bumps is only about several milli-ohms, which is much smaller than that of the interconnect lines. Therefore, the regular 2-point resistance measurement does not have the required sensitivity to detect damage evolution in solder bumps in EM test. Figure 3.3 shows the voltage measurement across a solder bump test structure using 2-point method when 1A current was applied. It can be seen that the voltage variation is over 20mV, corresponding to a resistance variation of over 20 milli-ohms. The variation comes mainly from two parts; the thermal noise induced by the contact potential voltage and the resistance change of the interconnect lines caused by the local temperature fluctuation.

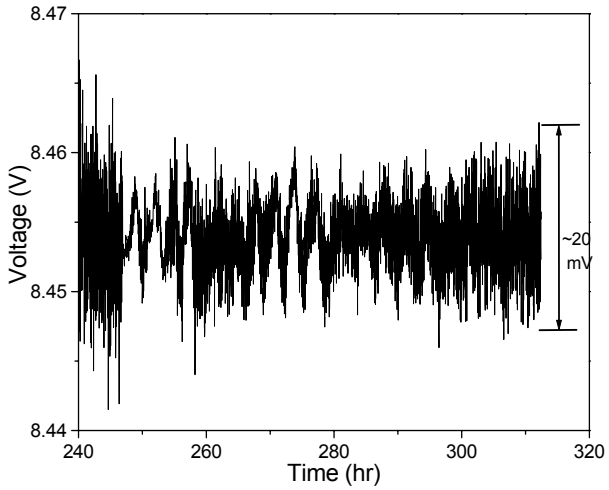


Figure 3.3 Voltage responses from solder EM test when 2-point resistance measurement is used

To reduce the measurement errors, a test methodology based on a Wheatstone bridge circuit was employed in this study. The method has been successfully applied in statistical studies of EM failures in interconnects [3.1, 3.2]. The bridge circuit, shown in Figure 3.4, consists of electrical current source and a voltmeter connecting two parallel branches containing four resistors. One branch contains a fixed resistor R1, and a variable resistor R2. Both values are in the order of 10^3 ohms. The other branch contains one pair of solder bumps, R3 and R4, whose resistance is about several milli-ohms. The bridge is balanced by carefully adjusting R2, setting the off-balance voltage V_g to be close to zero at the beginning of the test. During the test, EM damage in the solder bumps causes the resistance of R3 or R4 (but not at the same time) to increase, thus inducing an off-

balance voltage Vg. At the same time, thermal noise in both branches of the bridge will cancel each other out and make little contribution to Vg.

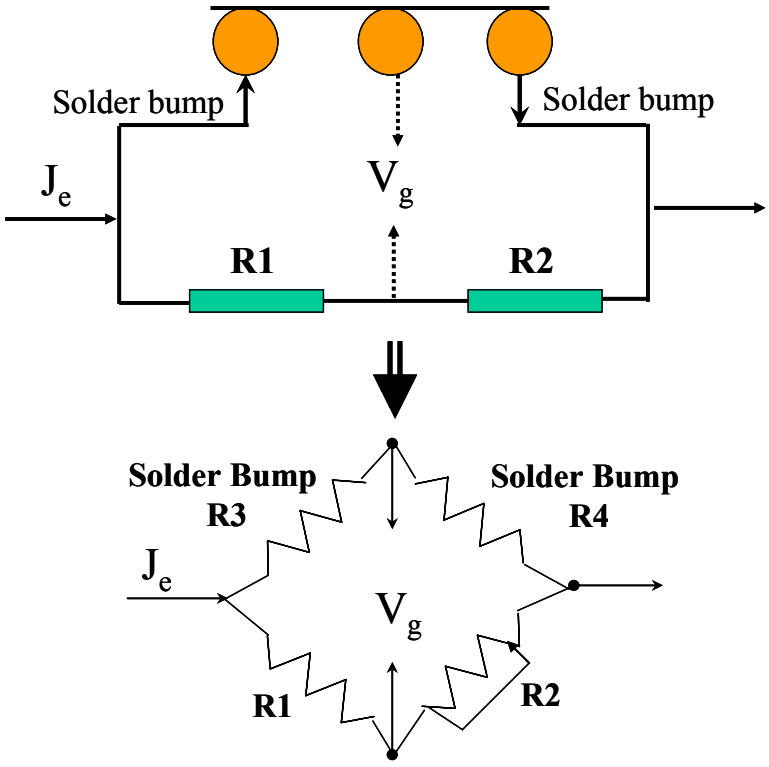


Figure 3.4 Schematic drawing of the Wheatstone bridge circuit used in solder EM test

V_g is used to determine the resistance change induced by EM damage in solder bumps. According to Kirchhoff's law, we can deduce V_g in the bridge circuit in Figure 3.4 as,

$$V_g = IR\left(\frac{R_3}{R_3 + R_4} - \frac{R_1}{R_1 + R_2}\right) \tag{3.2}$$

where I is the constant test current and R is the total resistance of the circuit,

$$R = \frac{(R_1 + R_2)(R_3 + R_4)}{R_1 + R_2 + R_3 + R_4} \tag{3.3}$$

Combining (3.2) and (3.3), R_4 is given by

$$R_4 = \frac{R_2 R_3}{R_1 - \frac{V_g}{I}} + \frac{V_g}{I}\frac{(R_1 + R_2 + R_3)}{R_1 - \frac{V_g}{I}} \tag{3.4}$$

and ΔR_4 is

$$\Delta R_4 = \frac{\partial R_4}{\partial V_g}\Delta V_g = \frac{\Delta V_g}{I} \cdot \frac{R_1 R_2}{(R_1 - \frac{V_g}{I})^2}(1 + \frac{R_1}{R_2} + \frac{R_3}{R_2} + \frac{R_3}{R_1}) \tag{3.5}$$

Similar formulae can be deduced for ΔR_3. Note that R_1 and R_2 are fixed and several orders of magnitude larger than R_4, and assuming that the resistance of bump R_3 remains constant (the reason will be discussed in the next chapter), ΔR_4 can be simplified as

$$\Delta R_4 \approx \frac{\Delta V_g}{I} \cdot (1 + \frac{R_2}{R_1}) \tag{3.6}$$

The off-balance voltage change is linearly related to the change of resistance in the solder ball. In Figure 3.5, a typical trace of V_g monitored from one EM test is shown. From the trace we can see that V_g continue to increase, indicating the evolution of EM damage in the solder bump.

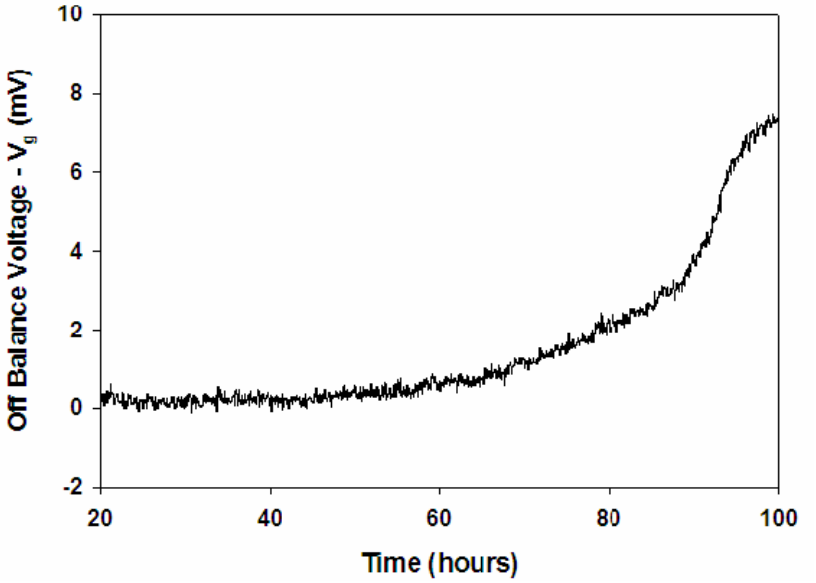


Figure 3.5 Typical V_g -T curve from solder EM test

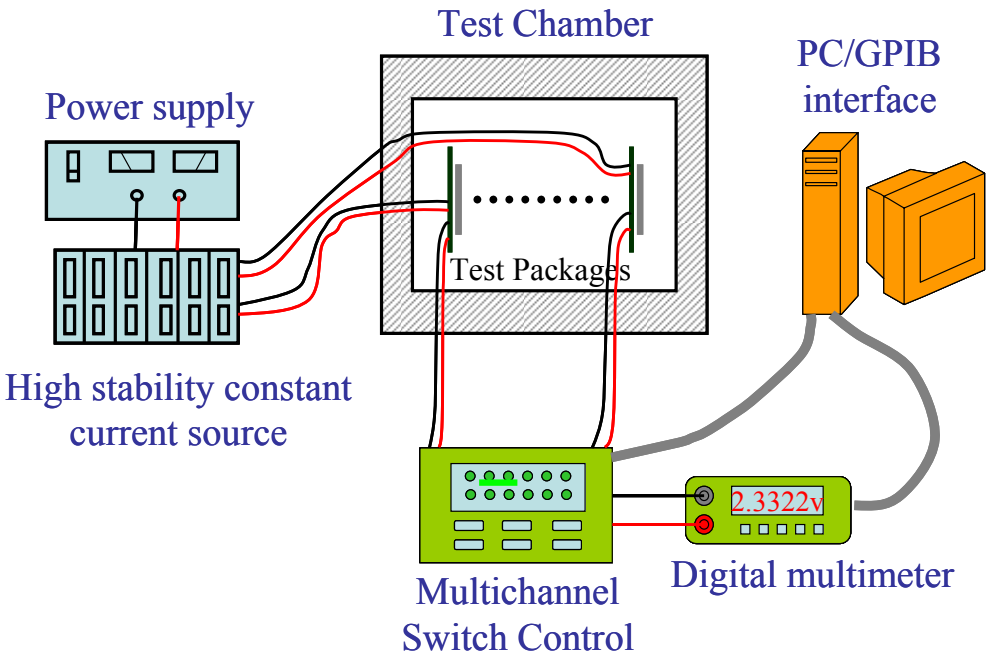


Figure 3.6 Schematic drawing of the solder EM test system

The high sensitivity of the Wheatstone bridge method backed up by a high stability current source enables a precise tracking of the evolution of electromigration damage in solder bumps and becomes the backbone of the test system. Other parts of system include the controlling computer, test chamber that can be heated up to 200^{o}C, switching box to test multiple samples at the same time. The schematic drawing of the entire test system is shown in Figure 3.6.

3.4 TEMPERATURE CALIBRATION

Electromigration tests are normally performed at elevated temperatures. Due to the Joule heating effect, the actual temperature of the test structure is normally higher than that of the ambient. The first attempt to check the temperature increase due to Joule heating was made by attaching a thermocouple on the top surface of the die, as shown in Figure 3.7. It was found that the temperature increase over ambient on the die surface of the sample was about

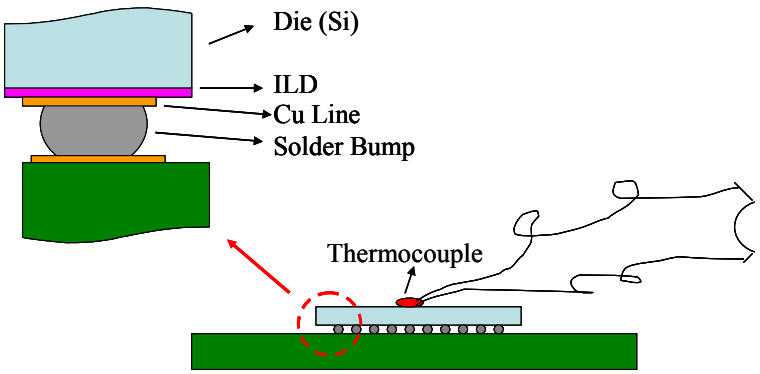


Figure 3.7 Measurement of Joule heating effect using thermocouple

20-40^{o}C when 1 A current was applied.

However, the temperature of the solder bump could be different from that of the die top because the inter-layer dielectric material (ILD) between the bump and the die, as illustrated in Figure 3.7, is not very thermally conductive and large temperature gradients could exist within it. Another way to determine the temperature of the solder bump is to track the resistance changes of the test interconnect structure which consists of the Cu lines on the die side, the solder bump and the Cu lines in the substrate. The resistance is directly related to the temperature as,

$$R = R_0(1+\alpha(T_D - T_0)) \quad \text{or} \quad T_D = \frac{1}{\alpha}(\frac{R}{R_0} - 1) + T_0 \tag{3.7}$$

where T_0 is the reference temperature (20^{o}C), R_0 is the resistance at T_0, α is the temperature coefficient of resistance (TCR) and T_D is the average temperature of the test structure. To understand the correlation between the temperature increases due to Joule heating, thermal analysis was performed for the test structure. The temperature increase over the ambient is,

$$\Delta T = (T_D - T_A) = \theta_{DA} P = \theta_{DA} I^2 R \tag{3.8}$$

where P is the power supplied, I is the test current, R is the resistance of the test structure, T_D is the temperature of the test structure, T_A is the ambient temperature and θ_{DA} is the thermal resistance between the structure and the ambient environment.

Combining (3.7) and (3.8), the resistance of the test structure in EM test is,

$$R = \frac{R_0(1+\alpha(T_A - T_0))}{1-\alpha\theta_{DA}I^2R_0} \tag{3.9}$$

Two parameters, α and θ_{DA}, control the thermal behavior of the test structure under different currents and ambient temperatures. The TCR was determined by measuring the resistance with increasing temperature at a minimal applied current (50 mA). The TCR was found to be $3.6\text{x}10^{-3}/^{o}\text{C}$ as shown in Figure 3.8, which was between those for bulk Cu ($3.9\text{x}10^{-3}/^{o}\text{C}$) and 0.5 μm wide Cu interconnects ($3.3\text{x}10^{-3}/^{o}\text{C}$) [3.3].

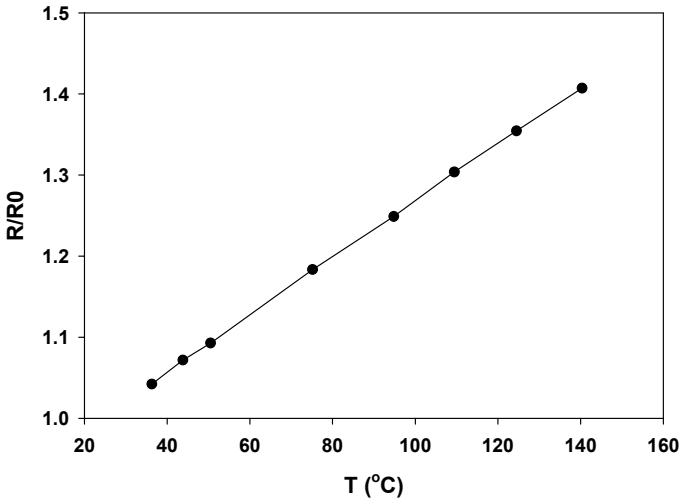


Figure 3.8 Test structure resistance change with temperature

The θ_{DA} was determined by applying a series of currents and measuring the resistance of the test structure after the temperature stabilized. Figure 3.9 shows the resistance-current behavior of a sample at an ambient temperature of 120°C. By fitting (3.9) to the experimental data, θ_{DA} was found to be 38°C/W.

The temperature increase of the sample under different current and ambient temperature can then be predicted using Eqs. (3.7) and (3.9) as shown in Figure 3.10.

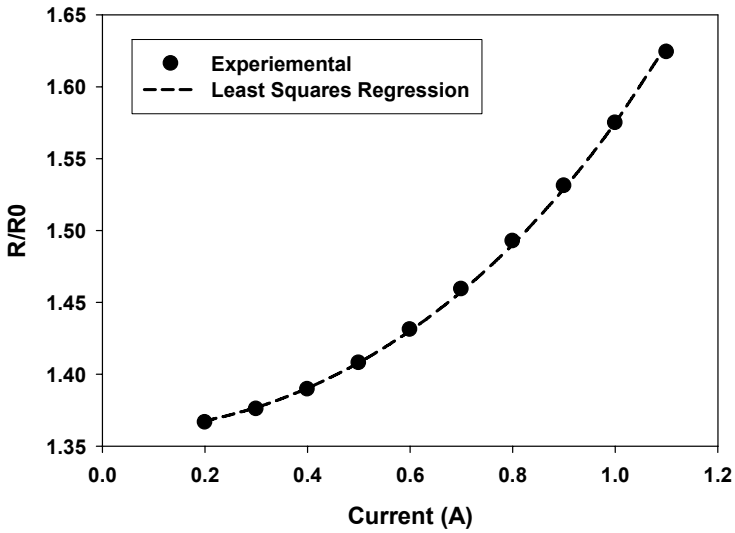


Figure 3.9 Test structure resistance change with current

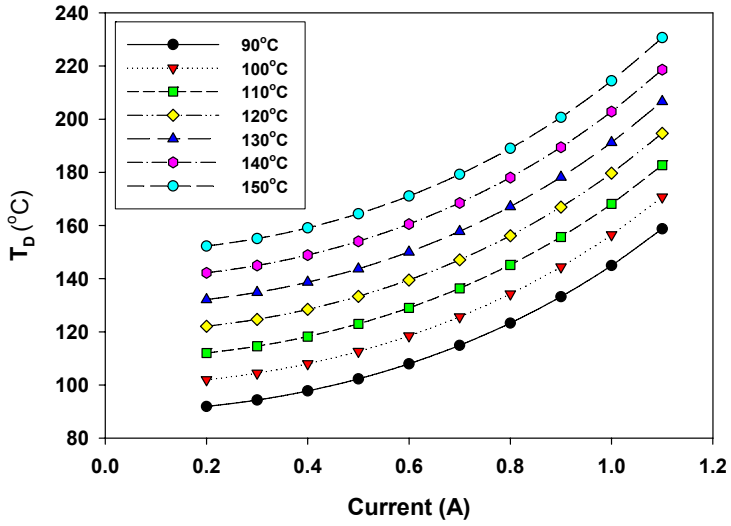


Figure 3.10 Calculated temperature change of the test structure under different current and ambient temperature

In order to compute T_D as the temperature of the solder bump under test, two assumptions have to be made,

1. The temperature gradient within the interconnect structure is reasonably small.
2. The resistance of the entire test structure comes mainly from the interconnect lines (die side and substrate side) and therefore a single α can be applied to calculate T_D.

Assumption 2 is reasonable for most cases because the interconnect lines in microelectronic packages are mainly made of Cu and the resistance of the Cu lines is much higher than that of the solder bump. However, Assumption 1 is realistic only if the packages have thick and wide interconnect lines.

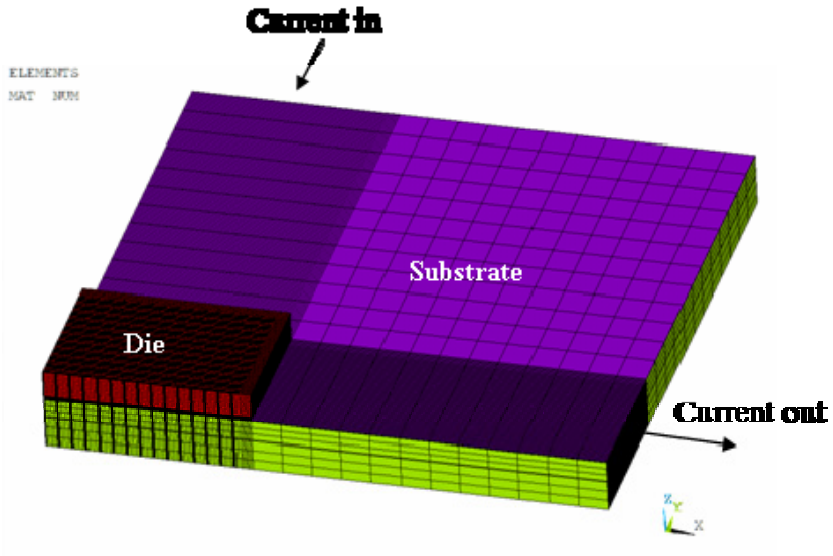


Figure 3.11 Three dimensional FE model for temperature estimation

To supplement the resistance monitoring method, the temperature distribution inside the test structure was estimated by finite element (FE) analysis. Three dimensional FE models were built using the ANSYS software. A quarter of the flip chip package of interest, as shown in Figure 3.11, was simulated based on symmetry to save computing resource. Adaptive meshing was used to generate dense mesh in the critical regions and coarse mesh in the rest of the model. A constant current was applied at both ends of the substrate Cu traces connecting the solder bumps. The die top temperature was set to be the value measured by thermocouples. Natural convection boundary conditions were applied to substrate surfaces. The material properties used in the simulation are listed in Table 3.1.

Table 3.1 Material Properties used in FE analysis [3.4, 3.5]

Component	k (W/m.^{o}C)	ρ (μΩ–mm)
Die	140	--
Dielectric layer	0.29	--
Underfill	0.55	--
Soldermask	0.26	--
Substrate	13	--
Cu	401	17
Al	235	27
Ni	70	91
Solder	51	143

One example of the analysis result is shown in Figure 3.12. It was found that a large temperature gradient (>40^{o}C) existed in the long thin interconnect lines in the substrate. In this case, FE analysis is necessary to obtain the temperature of the solder bump under test more accurately. It was also found that a 3~5^{o}C temperature gradient existed within the solder bump as shown in Figure 3.13.

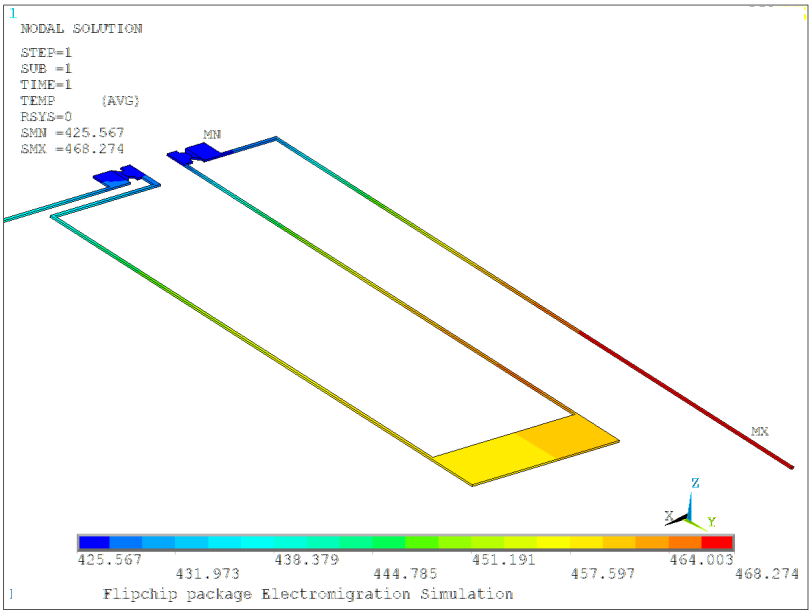


Figure 3.12 Temperature distribution in the Cu line by FE analysis

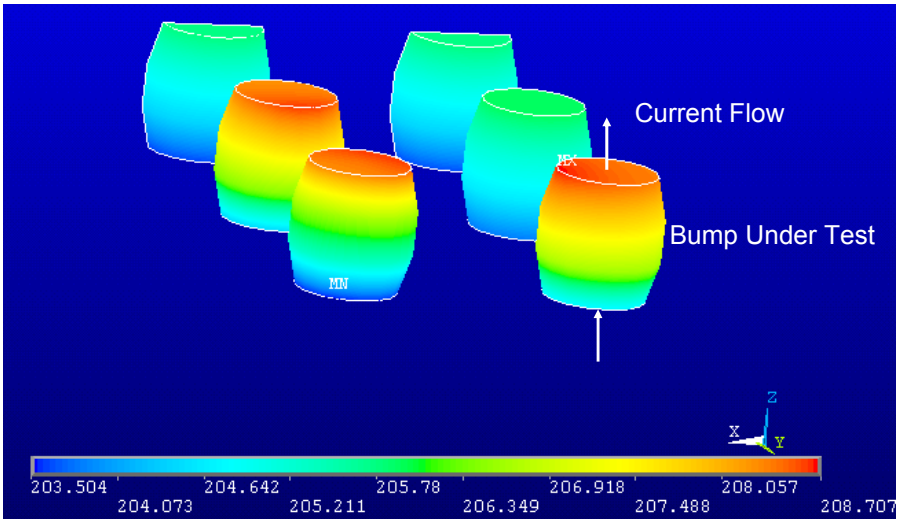


Figure 3.13 Temperature distribution in solder bumps from FEA simulation

3.5 STATISTICAL LIFETIME ANALYSIS

In a serial chain of interconnects, a "weak link" is the one that will fail earlier than any of the other links in the interconnect chain and will subsequently determine the reliability of this composite structure. In the case of a collection of identical and independently failing interconnects, a serial circuit of N interconnects will only function as long as the weakest interconnects does not fail. In such a case, the random failure time of the system $\boldsymbol{\tau}$ is given by

$$\tau = \min(\tau_1, \cdots, \tau_N) \tag{3.10}$$

where $\tau_1, \ldots, \tau_N$ are the potential random failure times from a population of N interconnects. Thus, the system failure is defined by the occurrence of first

failure in the ensemble and referred to as a "series system" or the Weakest Link Model [3.6-3.8]. In a system containing N independent elements, the system reliability (meaning the probability of system survival up to a time $\boldsymbol{t}$ is given by the product rule for serial systems:

$$R_N(t) = \prod_{i=1}^{N} R_{Ni}(t) \tag{3.11}$$

where $R_{Ni}(t)$ is the reliability of the ith of N independent components at time t and R_N(t) is the system reliability. Since $R_N(t)=1-F_N(t)$, one can deduce:

$$1 - F_N(t) = \prod_{i=1}^{N} [1 - F_{Ni}(t)] \tag{3.12}$$

where $F_N(t)$ is the cumulative probability of the system failure within the time interval (0,t]. If the $F_i(t)s$ are the same regardless of i, the above equation can be simplified as

$$F_N(t) = 1 - (1 - F_i(t)]^N \tag{3.13}$$

The last equation is the so-called Weakest Link Approximation *(WLA)*, and $F_N(t)$ is the cumulative distribution function (CDF) for a series of N independent but identical elements. The function $F_i(t)$ is the CDF for a single interconnect and, for the purposes of this study, is assumed to follow log-normal statistics.

It has been reported that the cumulative distribution function of failure (CDF) of a group of single interconnects can be fitted by a lognormal distribution [3.3, 3.6]. The log-normal probability density function of failure (PDF) is given by

$$f(t) = \frac{1}{\sigma t\sqrt{2\pi}} e^{\frac{-(\ln t - \ln t_{50})^2}{2\sigma^2}} \tag{3.14}$$

where t_{50} is the median time to failure and σ the standard deviation in log-time. The integral of the PDF from 0 to time t is the CDF, *F(t)*, which can be expressed using a Gaussian integral

$$F(t) = \int_0^t f(u)du = \frac{1}{(2\pi)^2} \int_{-\infty}^{z} e^{-\frac{v^2}{2}} dv \tag{3.15}$$

where z=[ln(t)- ln(t_{50})]/σ and t>0. The CDF describes the probability of an interconnect failing within the time interval, [0,t]. The inverse function, $F(t)^{-1}$, then gives the corresponding failure time window for a given probability value.

In this work, the values of cumulative probability of system failure $F_N(t)$ at different times, t_i, can be obtained experimentally from the sample lifetime by

$$F_N(t_i) = \frac{i - 0.3}{N_{total} + 0.4} \tag{3.16}$$

where *i* is the index of the sample after all the samples were sorted by time to failure and N_{totoal} is the total number of samples. At the same time, by combining (3.13) and (3.14), $F_N(t)$ can also be calculated for a given set of

samples. A computer program was written using a least square algorithm to find the combination of t_{50} and σ that could best fit the experimental data from (3.16). Figure 3.14 gives an illustration of the lifetime distribution of a 2-link test structure and the de-convoluted (N=1) lifetime distribution.

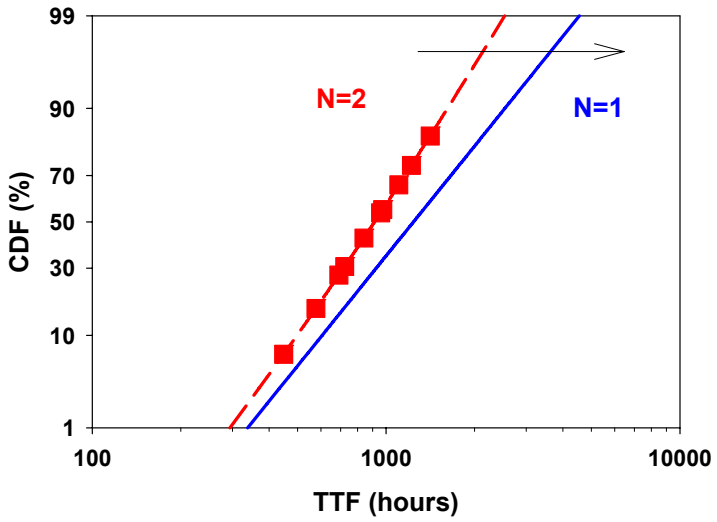


Figure 3.14 Lifetime de-convolution of multilink samples (N=2)

Chapter 4: Electromigration Study in Pb-free Solder Bump

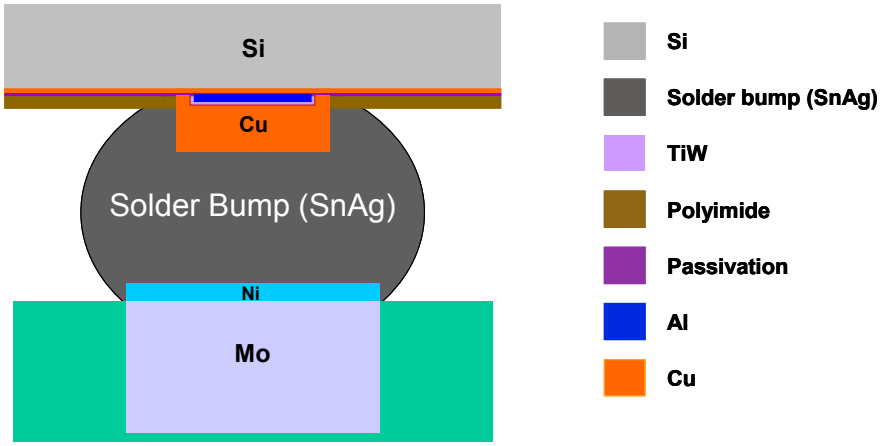
4.1 OVERVIEW

The RoHS (Restriction of Hazardous Materials) directive from the European Union requires the elimination of lead from electronic assemblies by July of 2006. Therefore, the implementation of Pb free solder alloys in microelectronic packages has been greatly accelerated in the past few years. Most of the Pb-free alloys targeted as the replacement of the SnPb solder alloy for flip chip packages are Sn based with small amount (usually less than 10%) additives such as Ag, Cu, Ni, In, etc. Since Sn is the primary element that reacts with the under bump metallurgy (UBM), it can be expected that the Pb-free alloys will consume the UBM at a faster rate with increased Sn content. The electromigration process may also be affected. In this chapter, the electromigration study of flip-chip packages with Pb-free solder bumps is reported.

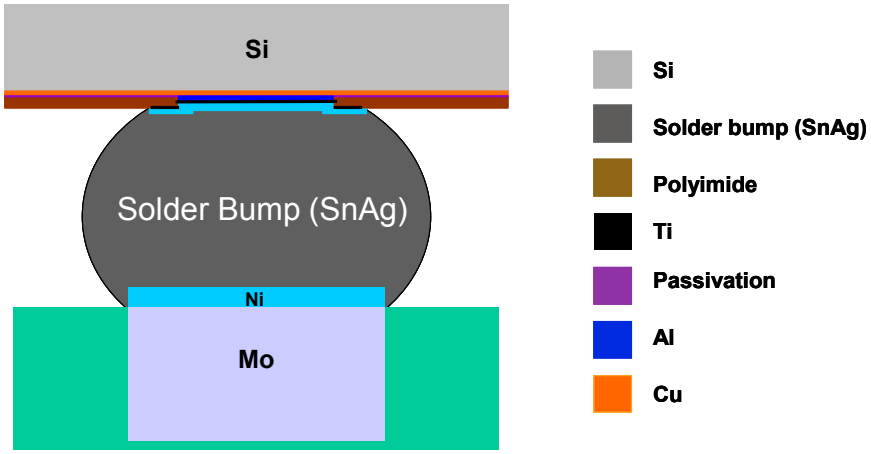
4.2 EXPERIMENTAL SETUP

EM tests were performed on 97.5wt%Sn-2.5wt%Ag (Sn-2.5Ag) solder bumps in flip chip package with ceramic (alumina) substrates. The structures of the solder bump tested are shown in Figure 4.1. The Sn2.5Ag solder bump had a nominal diameter of 130 μm and height of 60~80μm. The passivation opening was 55μm. Two different designs of under bump metallization (UBM) were chosen. One had a 0.25μm-TiW/18μm-Cu UBM, and the other had a 0.1μm-

Ti/2μm-Ni. Thickness variations of Cu and Ni UBM were ±4 μm and ±1 μm, respectively. On the substrate side, the solder pad was Cu with 5μm electrolessly plated Ni(P).



(a)



(b)

Figure 4.1 Structure of Solder Bump: (a) Cu-UBM (b) Ni UBM

A Wheatstone bridge circuitry was used, as described in chapter 3, to detect the small resistance change in sold bumps during electromigration tests. Two pairs of solder bumps in the same flip chip package were connected to form one branch of the Wheatstone bridge, as shown in Figure 4.2, making it a two-link (N=2) test structure. In each pair of the joints, the *cathode bump* refers to the solder bump in which the direction of electron current is from the substrate to the die, and the *anode bump* refers to the bump with the opposite direction of electron current. After assembly, the gap between the die and the substrate was underfilled. To start the EM test, the off-balance voltage V_g in the Wheatstone bridge circuit was set to zero by adjusting the variable resistor R_2. The value of V_g was directly correlated with the net resistance change of solder bumps only. In the test setup, R_1 and R_2 are kept constant and $R_1 \approx R_2 >> R_3 \approx R_4$. Therefore, (3.2) can be simplified to

$$V_g = 0.5I(R_3 - R_4) \tag{4.1}$$

During the EM test, R_3 and R_4 will increase due to EM induced damage. From (4.1), one can see that an increase of R_3 will cause V_g to be positive while the increase of R_4 will cause V_g to go negative. In this way, the V_g change can be used to track the net difference between R_3 and R_4. Because the timeframe for one bump to fail is quite short (<1 hour) compared with the test time (10~10^3 hours), there is little chance that the other pair of bumps will fail at the same time. Since the two pairs of bumps are connected serially, the open circuit failure of one pair will bring the current to zero, leaving the test of the other pair intact. Therefore,

the lifetime of only half of the population was collected during the test. To obtain the statistics of the whole population, we need to apply the weakest link approximation analysis.

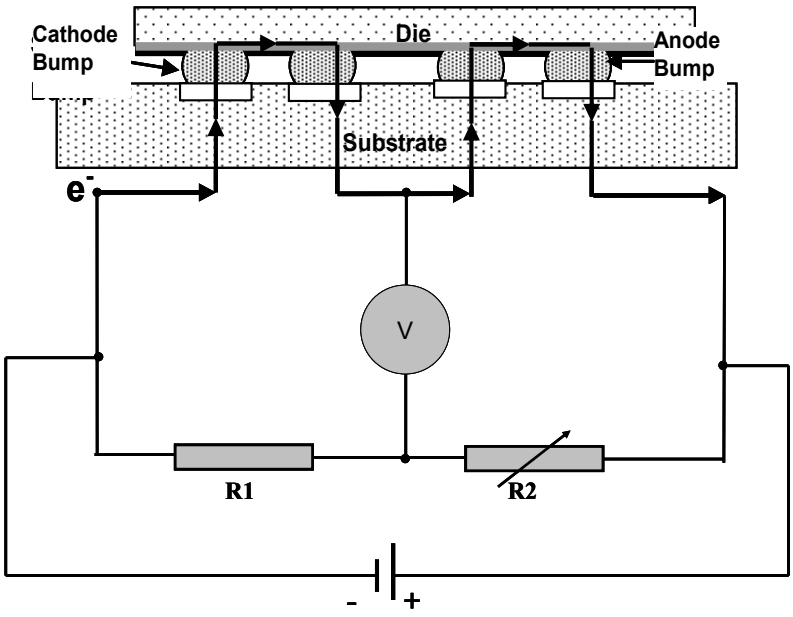


Figure 4.2 Cross-section of solder bump pair under test and test circuitry

During electromigration testing, the samples were heated in an oven. The Joule heating induced by the applied current was checked by attaching a thermocouple to the top of the die and compared with the temperature of the ambient temperature of the oven. In this way, Joule heating was found to increase the test temperature by about 20-30°C. A finite element thermal analysis showed that the temperatures of the solder bumps under test were 10~15^{o}C higher that of the die top. Three EM tests were performed with ambient temperature 90^{o}C,

105°C and 120°C, respectively. For the 90°C and 105°C runs, the current density was $3.5x10^4 A/cm^2$. For the 155°C run, the current density was $4.1x10^4 A/cm^2$. The current density was calculated by dividing the applied current by the area of passivation opening on the silicon chip. All test conditions are listed in Table 4.1.

After electromigration testing, selected packages were cross-sectioned and polished to the mid-plane of the tested balls for failure analysis. Backscatter electron imaging mode of scanning electron microscopy (SEM) was applied to examine the morphology of the solder bumps. Energy-dispersive x-ray spectroscopy (EDS) was used to determine the composition of the intermetallic compounds.

Table 4.1 Test conditions of the EM test

Temperatures	Ambient (Oven) (°C)	90	105	120
	Die Top (°C)	110	122	155
	Solder Bump (°C)	120	132	170
Current Density (A/cm^2)		$3.5x10^4$	$3.5x10^4$	$4.1x10^4$

4.3 CURRENT CROWDING IN SOLDER BUMPS

As the electrons flow in the thin film interconnect on the die side and approaches the edge of solder bump, electron current divergence occurs (see Figure 4.3). The electrons enter the solder bump at the passivation opening edge, creating a localized high current density called current crowding. Since the rate of

electromigration damage is dependent on the current density, the current distribution inside the sample needs to be examined in order to understand the electromigration damage evolution.

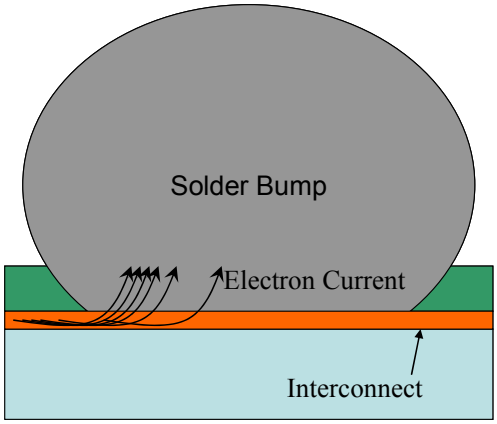
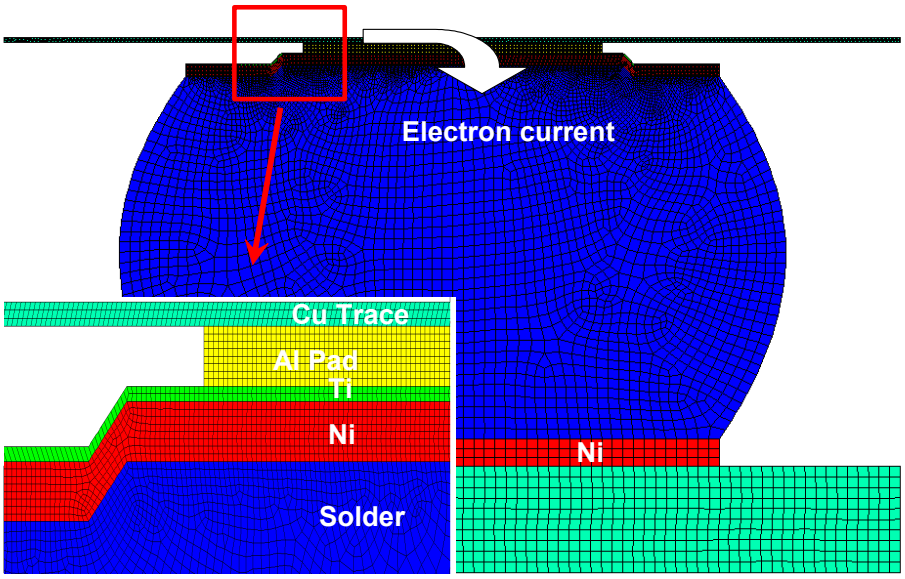


Figure 4.3 Current flow pattern at the solder-interconnect interface

Two-dimensional finite element models were built for both Ni-UBM and Cu-UBM samples (Figure 4.4). The simulation results of the current distribution in the solder bumps are shown Figure 4.5. In this simulation, a nominal current density of $1.1 \times 10^4/cm^2$ (based on maximum bump diameter) was applied. For Ni-UBM samples, the current crowding region was very close to the edge of the passivation opening where the current deviated from the interconnect line into the solder. The current density in the current crowding region was about 4~5 times higher than the average density. For Cu-UBM samples, the current crowding region extended to the entire perimeter of the thick Cu-layer due to the good electrical conductivity of Cu. The maximum current density was reduced to about 2~3 times higher than the average density.



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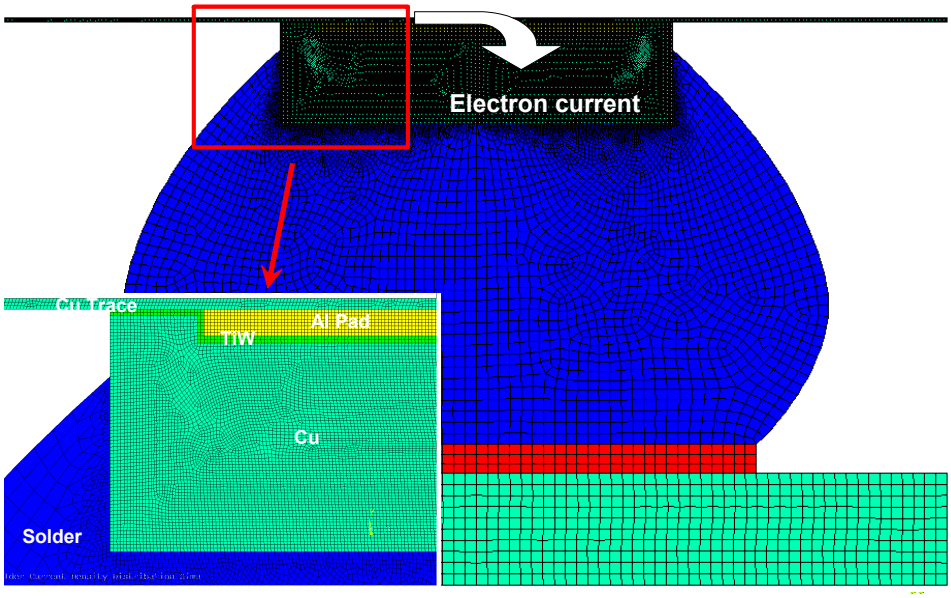
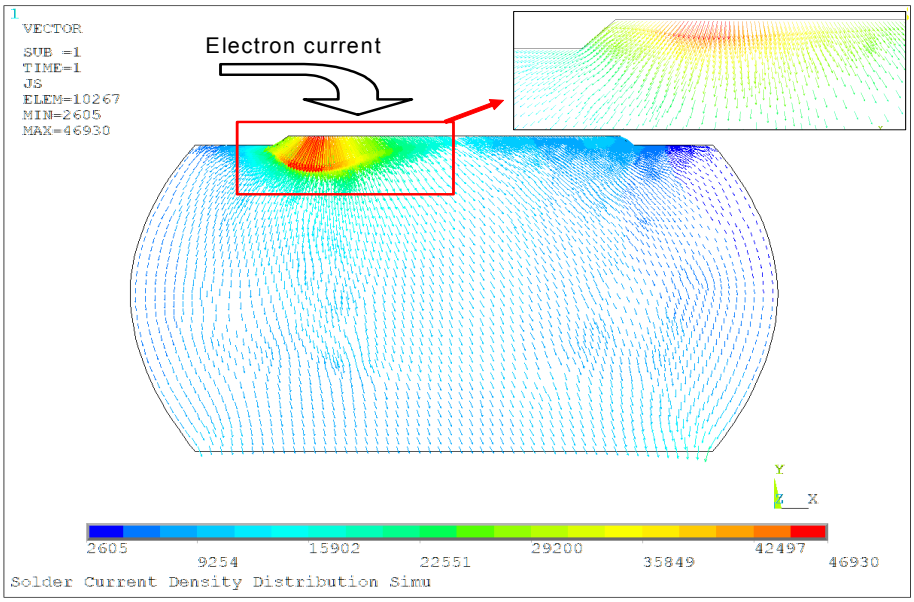
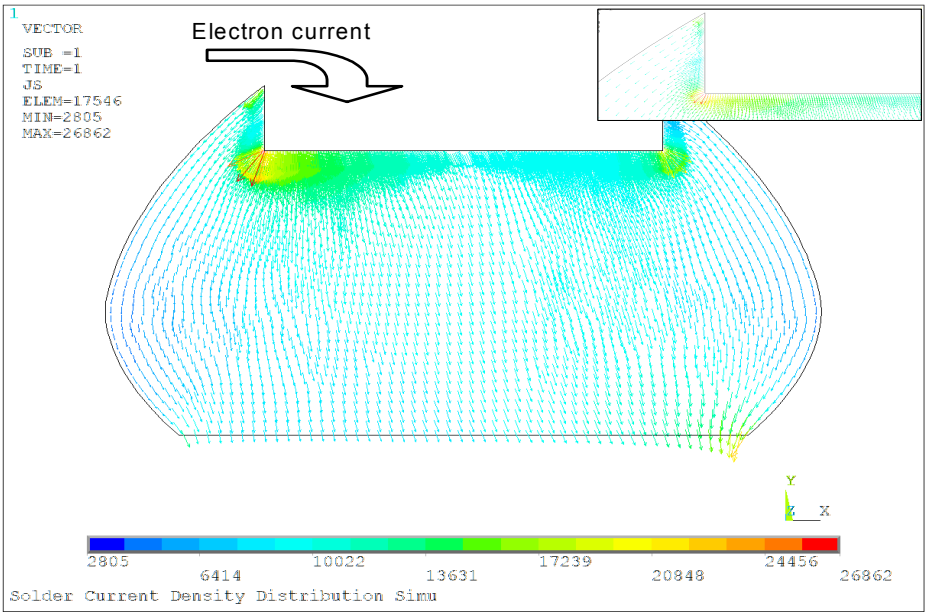


(b)

Figure 4.4 FE model of the solder bump with (a) Ni UBM; (b) Cu UBM



(a)



(b)

Figure 4.5 Current distribution in the solder with (a) Ni UBM; (b) Cu UBM

4.4 FAILURE MECHANISM ANALYSIS

To trace the damage evolution, samples were taken out of the oven at different times and cross-sectioned. Next, they were then examined with SEM/EDS. Open circuit failures are found to be at the die side of the *anode bumps* for both types of samples, where the electron current flows from die to substrate.

4.4.1 Failure Analysis - Ni UBM Samples

Bumps without current: SEM image of a solder bump annealed at 120^{o}C ambient temperature is shown in Figure 4.6. Significant growth of intermetallic layer was observed compared with T0 samples due to the interdiffusion and reaction of Ni and Sn. EDS analysis showed that the intermetallic was Ni_3Sn_4 on the die side and Ni_3Sn_4+ Ni_3P on the substrate side. No voids were observed in the intermetallics and the solder joint maintained its structural integrity.

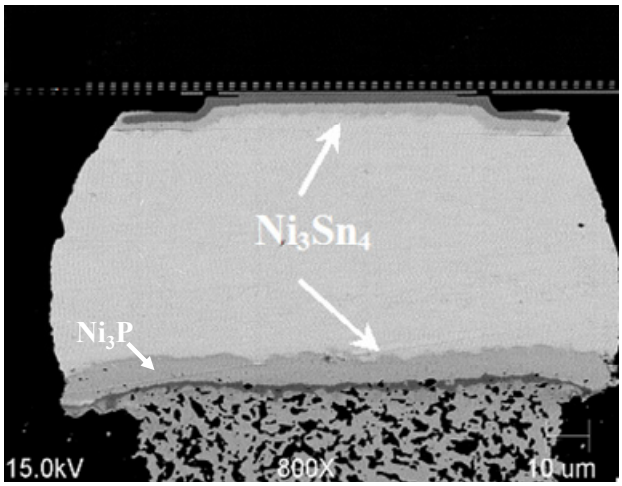


Figure 4.6 SEM image of Ni-UBM solder bump without current stressing at 120^{o}C after 250 hours

Anode bumps with Ni UBM: Figure 4.6 shows the SEM images of the *anode bumps* (90^{o}C ambient) at different stages of the test. From Figure 4.7(a), one can see that Ni UBM is continuous and no structural damage is apparent, e.g. delaminations or cracks could not be found at the beginning of the test. During the EM test, Ni_3Sn_4 was found to build up irregularly at the substrate side, as shown in Figure 4.7(b). This indicates that, driven by electron current, Ni atoms migrated away from UBM toward the substrate side. The depletion of Ni leaves vacancies in the depleted area and the concentration of the vacancies is proportional to the current density. Consequently, as shown in Figure 4.7(d), the corner of the solder bump with the maximum current density had the highest vacancy density. The agglomeration of the vacancies leads to the nucleation of a macro void. Once the void was nucleated, it became a sink for the lattice vacancies in the solder. The void then propagated along the solder/intermetallic interface with the vacancies diffusing along that interface to the void, as described in chapter 2 and shown in (Figure 4.7(e)). Figure 4.7(c) shows that the void propagation has delaminated the entire solder/intermetallic interface causing an open circuit failure.

Failure analysis of samples from the 120^{o}C test revealed a different failure mode as shown in Figure 4.8. It can be seen that not only was the Ni UBM almost completely consumed, but also the intermetallic compound disappeared from the die side. Since the Ni and intermetallic compound served as the adhesion layer between the solder and the Ti layer, disappearance the IMCs caused the solder to separate from the die side and caused open circuit failure.

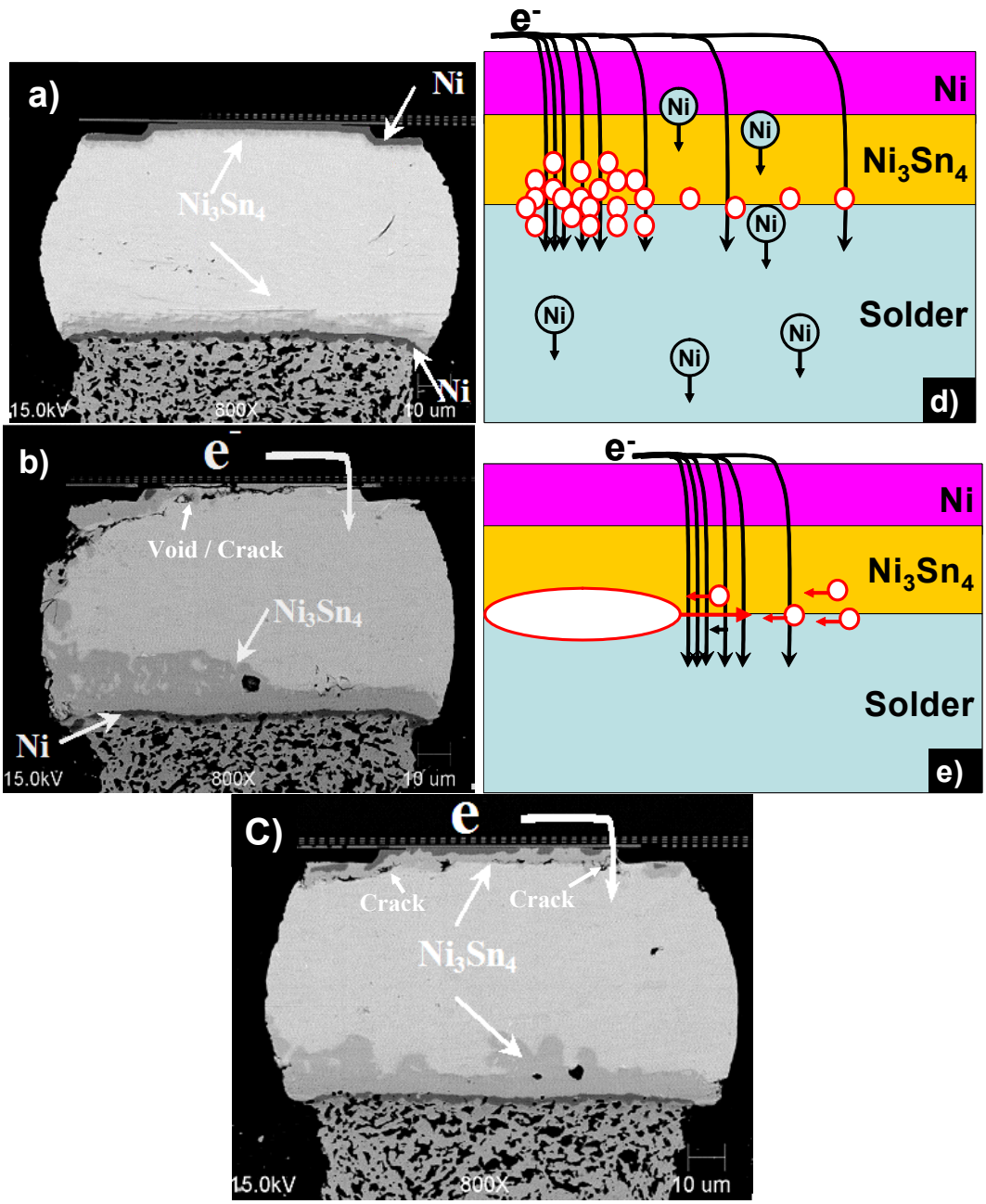


Figure 4.7 EM damage evolution of Ni-UBM samples at 110°C (a) t=0; (b) t=1000 hrs; (c) t=1400 hrs ; (d) lattice vacancy formation induced by electron current; (e) void formation and propagation at solder/intermetallic interface

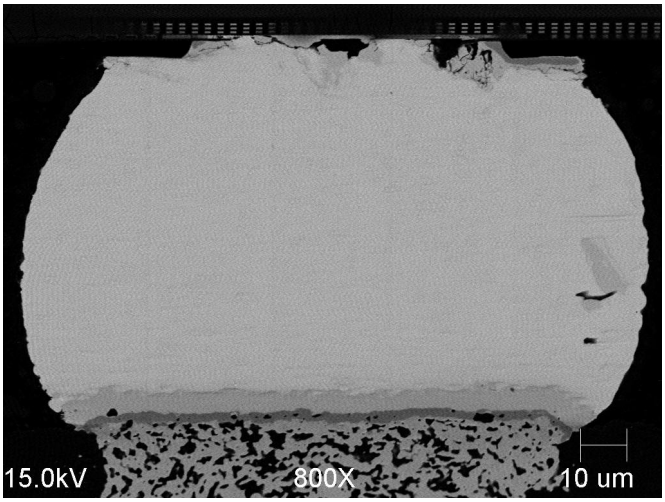


Figure 4.8 EM damage evolution of Ni-UBM samples at 110^{o}C

Cathode bump: Although all the open circuit failures were found at the UBM side of *anode bumps*, EM damage (voids and small cracks) was also seen at the substrate side in some of the *cathode bumps* for both Cu and Ni UBM samples. As shown in Figure 4.9, Ni atoms from the substrate cladding migrated upwards to the die side driven by the electron current and formed IMC. The thickness of the substrate cladding was greatly decreased. Small voids could also be found at the substrate solder interface due to the depletion of Ni. However, no open circuit failures were observed. Compared with the *anode bumps*, the more uniformly distributed current from the via underneath the bump helped to reduce current concentration and reduced the accumulation of vacancies.

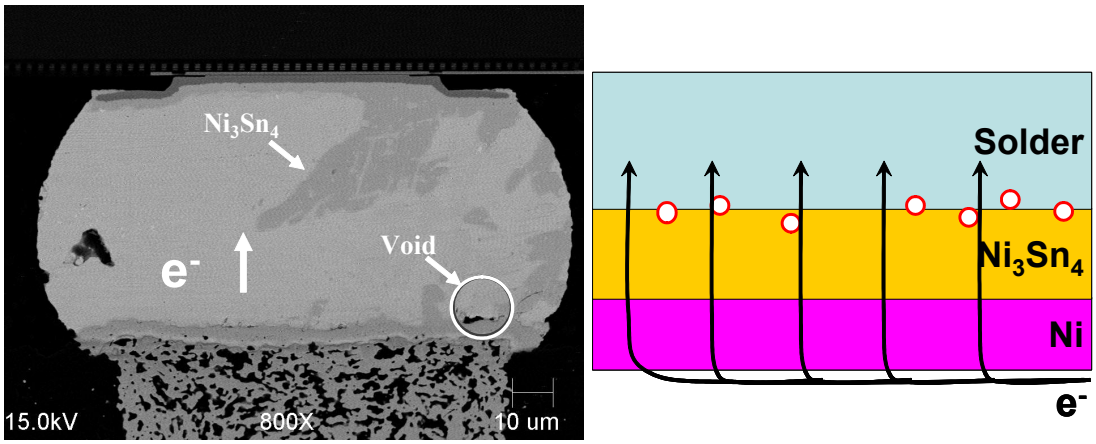


Figure 4.9 EM damage in cathode side bump (Ni UBM)

4.4.2 Failure Analysis - Cu UBM Samples

Bumps without current: SEM image of a solder bump annealed at 120°C ambient temperature is shown in Figure 4.10. On the die side, Cu_6Sn_5 and Cu_3Sn were observed between the Cu UBM and the solder as predicted by the phase diagram. Kirkendall voids are visible inside the Cu_3Sn layer and at the interface between Cu_3Sn and Cu. With continued annealing, the Cu_6Sn_5 and Cu_3Sn layers were found to grow with increased amount of Kirkendall voids. However, the voids were mostly isolated from each other without forming a continuous crack that could cause an open circuit failure. On the substrate side, $(Ni_x, Cu_{(1-x)})_3Sn_4$ ($x \approx 1$) was observed between the Ni(P) finish and the solder, indicating that a small amount of Cu migrated from the UBM to the substrate side. The thickness

of the $(Ni_x, Cu_{(1-x)})_3Sn_4$ also increased with annealing time, but at a much slower rate compared with the Cu_6Sn_5 and Cu_3Sn layers.

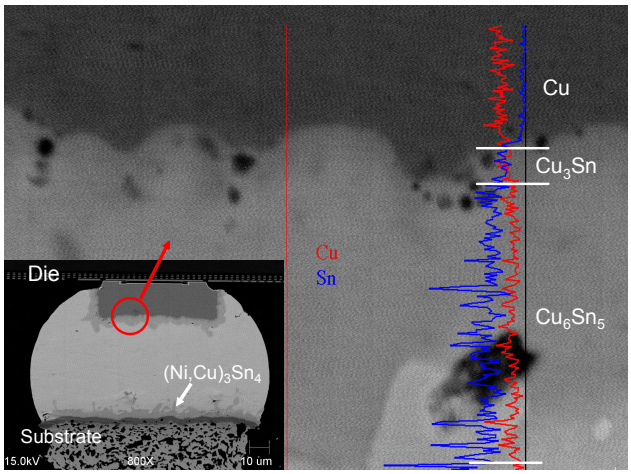


Figure 4.10 SEM image of the solder bump without current stressing at 120°C after 130 hours

Anode bumps with current stressing: When an electric current was applied, microstructural changes in the solder bump were significantly different than without current stressing. Two different damage evolution processes, I and II, were observed. Typical SEM images of the anode bump from different stages of the two processes are shown in Figure 4.11 and 4.12, respectively. Process I was observed more often at higher testing temperatures (105 and 120°C ambient). As the EM test continued, the Cu atoms from UBM migrated away driven by electron current and thus induced the dissolution of UBM, as shown in Figure 4.11(b). The Cu atoms accumulated at the substrate side forming intermetallic (Cu_6Sn_5) since the solubility of Cu in solder is rather limited. Finally, when most

of the Cu layer was dissolved, the solder separated from the TiW layer since Sn and TiW do not bond with each other (Figure 11(c)) and caused open circuit failure. Before the Cu layer was completely consumed, no interfacial crack was observed even though small voids could be seen to grow between the intermetallic layers Cu_3Sn/Cu_6Sn_5 on the die side.

Process II, as shown in Figure 4.12, was observed more often at lower testing temperatures (90^oC and 105^oC). The dissolution of the Cu layer in the UBM was not as significant as with process I when the solder bump showed open circuit failure (Figure 12(c)). During the EM test, voids nucleated from different sites in the intermetallic layers as shown in Figure 4.12(b). The voids propagated along the Cu_3Sn/Cu_6Sn_5 interface and finally caused an open circuit failure (Figure 4.12(c)).

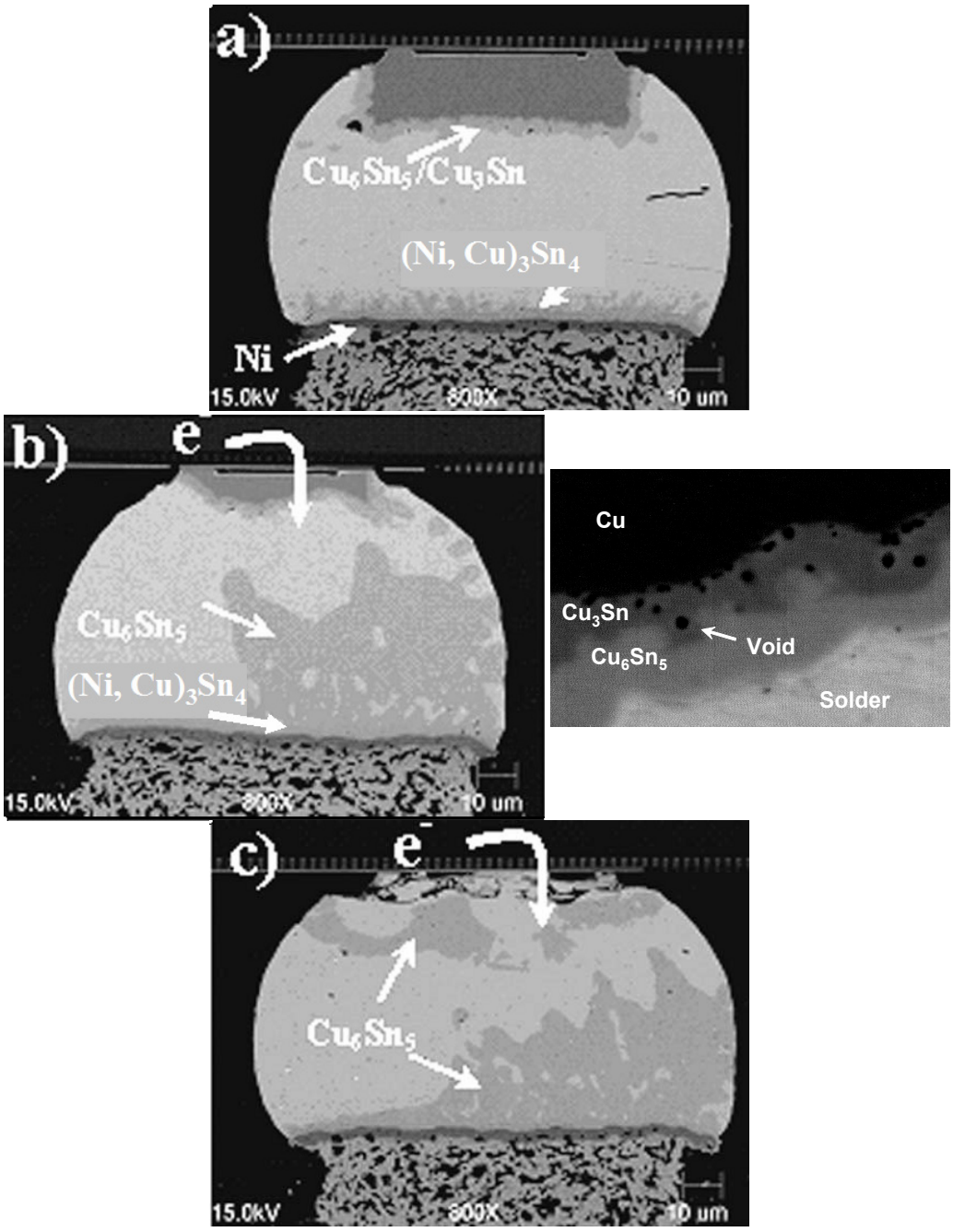


Figure 4.11 Cu-UBM samples with EM damage evolution type I (at 120°C)
(a) t=0; (b) t=60 hrs; (c) t=92 hrs

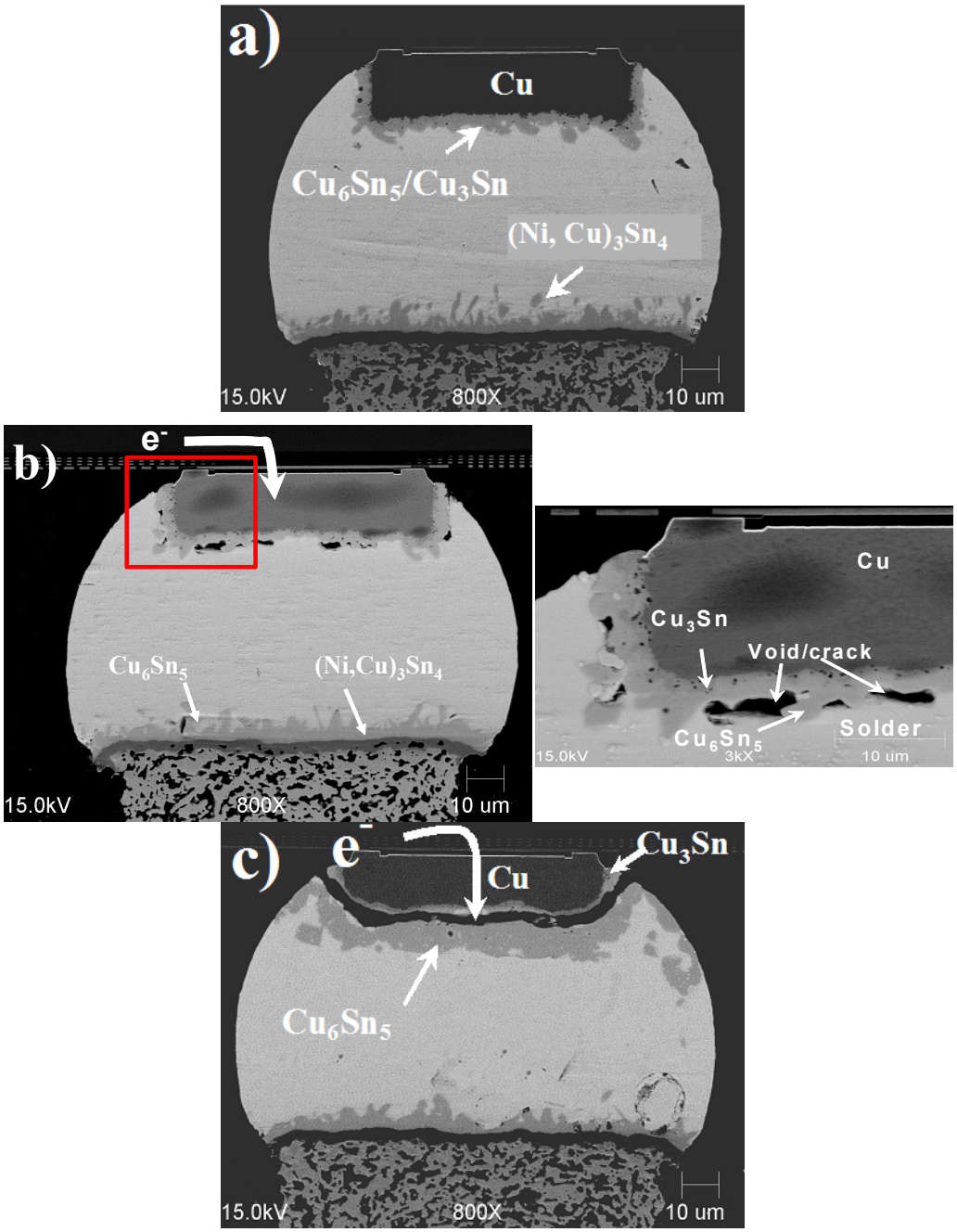


Figure 4.12 Cu-UBM samples with EM damage evolution process II (at 90°C) (a) t=0; (b) t=1000 hrs; (c) t=1400 hrs

One possible explanation for the temperature dependence of the EM damage process is illustrated schematically in Figure 4.13. At the beginning of the test, Cu_3Sn and Cu_6Sn_5 layers exist at the interface between Cu and solder (Figure 4.13(a)). During the EM tests, Cu atoms, driven by the electron current, diffuse from the Cu layer through Cu_3Sn and Cu_6Sn_5 into the solder, resulting in a reduction of the Cu layer thickness and the growth of the Cu_3Sn and Cu_6Sn_5 as shown in Figure 4.132(b). The interfaces of Cu/Cu_3Sn and Cu_3Sn/Cu_6Sn_5 then move toward the Cu side. At the same time, vacancies are accumulated at a location behind but very close to the receding Cu_3Sn/Cu_6Sn_5 interface [4.1].

When the vacancy density is high enough, voids will nucleate and start to grow along the interfaces between the two intermetallic layers with a mechanism similar to that of the Ni-UBM. The time between the beginning of the test and the nucleation of the voids is the void incubation time (t_{incu}). The difference between t_{incu} and the time for the Cu layer to be completed consumed (t_{Cu}) determines the failure mode. As shown in Figure 4.13(c), if $t_{incu} << t_{Cu}$, then the growth of the interfacial void will cut the diffusion path of Cu and preserve the Cu layer. If $t_{incu} >> t_{Cu}$, then the Cu_3Sn layer will reach the TiW layer and induce delamination since Cu_3Sn will not bond with TiW (Figure 4.13(d)). The failure analysis results of Cu-UBM indicate that t_{incu} is shorter than t_{Cu} at lower temperature and longer than t_{Cu} at higher temperature. The existence of the interfacial cracking failure mode at low temperature suggests that increasing the thickness of Cu may not necessarily improve EM performance for Pb free solder bumps with Cu UBM.

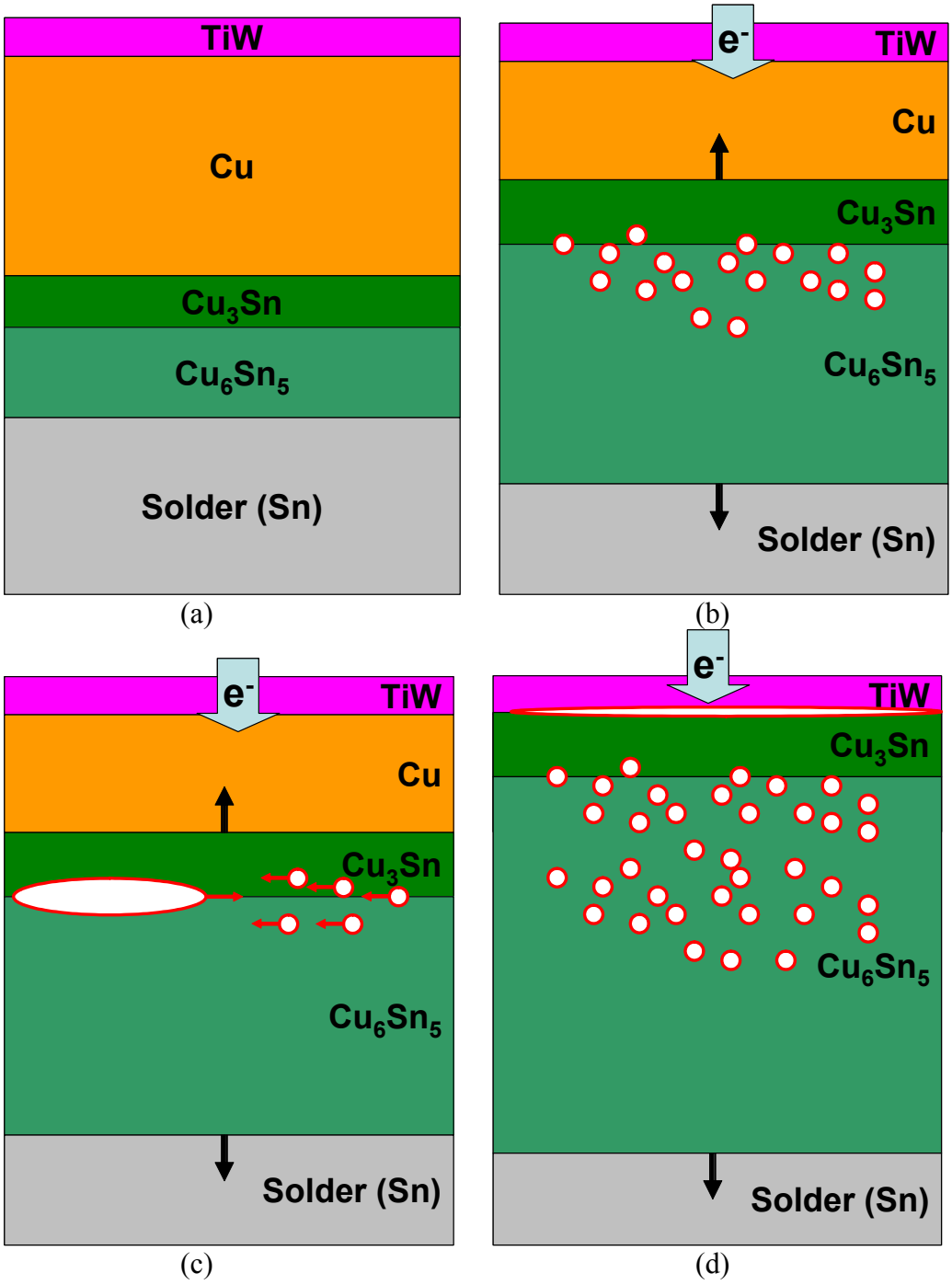


Figure 4.13 Illustration of the two EM failure modes of Cu-UBM sample

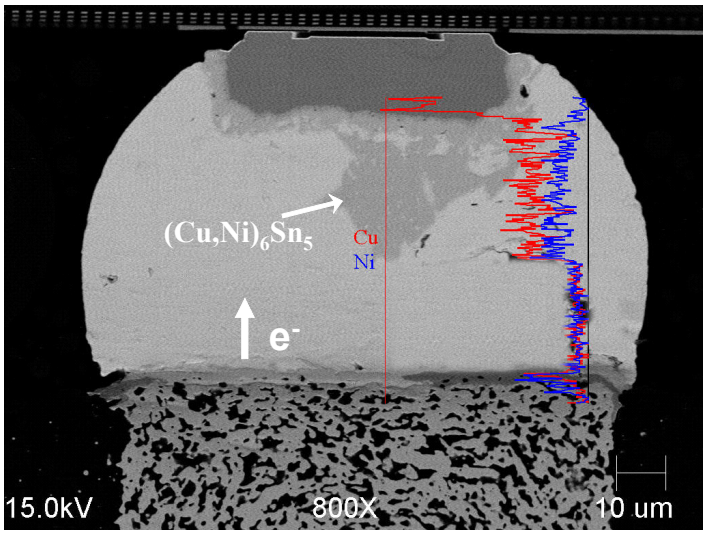


Figure 4.14 EM damage in a cathode side bump (Ni UBM)

Cathode bump: In the *cathode* bump (Figure 4.14), Ni atoms migrated from the substrate side to the die side and formed $(Cu,Ni)_6Sn_5$ phase inside the solder. The Cu atoms in $(Cu,Ni)_6Sn_5$ could have come from the UBM that was dissolved into the solder during reflow and the Cu atoms diffused from the UBM. At the Cu UBM/solder interface, the Cu_3Sn layer grew thicker under current stressing. The density of Kirkendall voids also increased but the density difference with and without current stressing was not so clear. At this point, most of the Kirkendall voids were still located in the Cu_3Sn layer near the UBM/ Cu_3Sn interface while the Cu UBM continued to be depleted. This indicates that Sn atoms were driven by current through the IMC layers to react with Cu atoms while Cu atoms diffused into solder in the direction opposite to the electron flow.

Without Sn diffusion, the additional depletion of Cu UBM cannot be explained as compared with the case without current stressing.

4.5 INTERMETALLIC COMPOUND GROWTH RATE

Figure 4.15 plots the nominal thickness of each IMC in anode joints as a function of time and temperature. The nominal thickness was calculated by dividing the cross-sectional area of each IMC with the original width of the corresponding UBM. The IMC thickness was fitted linearly with respect to time for simplicity, as shown in Figure 4.15. Table 4.2 listed the volume change during the formation of Cu_6Sn_5, Cu_3Sn and Ni_3Sn_4. A negative value of volume change means that the molar volume of the intermetallic compound is less than that of the mixture of the corresponding atoms. In this study, the IMC growth rate was found to follow the order of $Cu_6Sn_5 > Ni_3Sn_4 > Cu_3Sn$. Because Cu_6Sn_5 grew several times faster than the other two IMCs, the overall tensile stress caused by the formation of a large amount of Cu_6Sn_5 could be significant although its molar volume change is the smallest of the three IMCs. In contrast, a relatively small amount of Ni_3Sn_4 formation would have a large effect on EM damage since both the accompanying molar volume shrinkage and its Young's modulus are the largest of the three IMCs [4.2-4.4]. Continuous growth of IMCs enhanced by electric current increased the tensile stress with time, leading to significant driving force for crack propagation. Thus IMC growth is one of the key factors controlling EM reliability of Pb-free solder bumps.

Table 4.2 Volume change during intermetallic compound formation

	Cu_6Sn_5	Cu_3Sn	Ni_3Sn_4
Volume Change (%)	-5.2	-7.6	-11.4

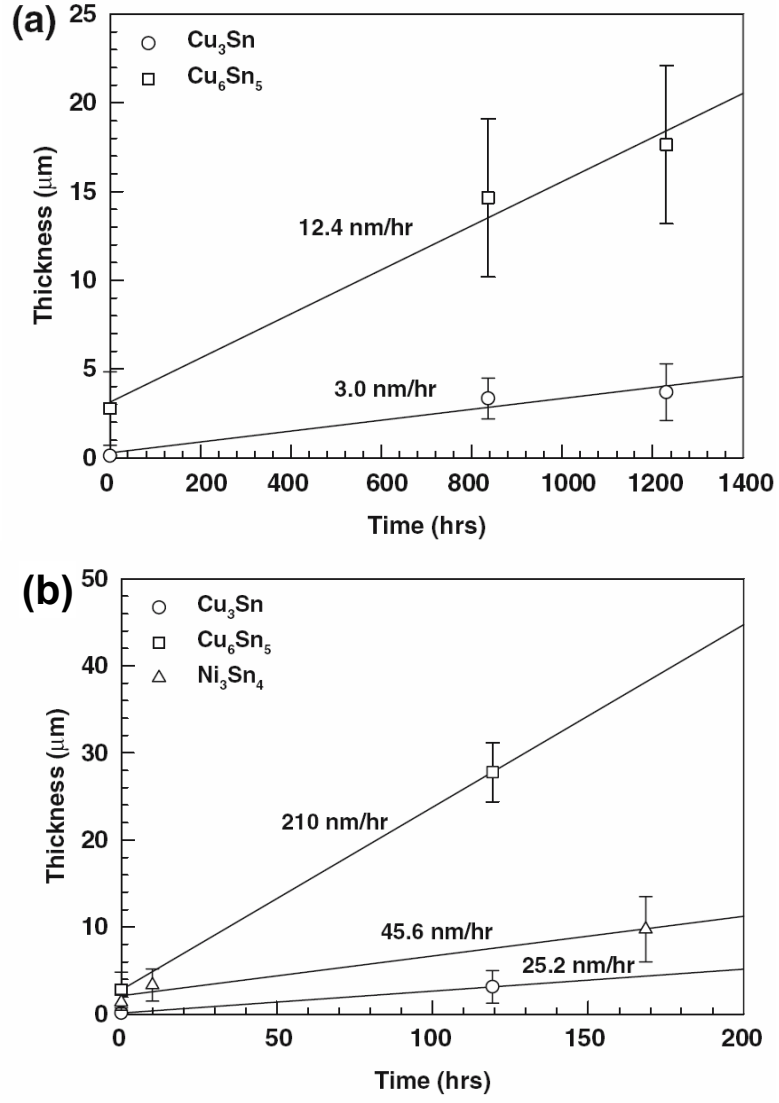


Figure 4.15 Intermetallic compound growth in EM test at (a) 105°C; (b) 120°C

4.6 LIFETIME STATISTICS

4.6.1 Lifetime Determination

In section 4.4, we discussed that the electromigration can induce cracks propagating along certain interfaces at the die side. A simple analytical model and an FEA model were set up to correlate the resistance change measured by the Wheatstone bridge method to the damage progress. The analytical model is shown in Figure 4.16(a). The solder bump is simplified as a block with cross-section area of $D_0 \times D_0$ and a height of h. The Cu interconnect lines has the same width as the solder block and with a thickness of t. The resistivity of the solder and Cu is ρ_{solder} and ρ_{Cu} respecitively. The initial resistance of the solder block is,

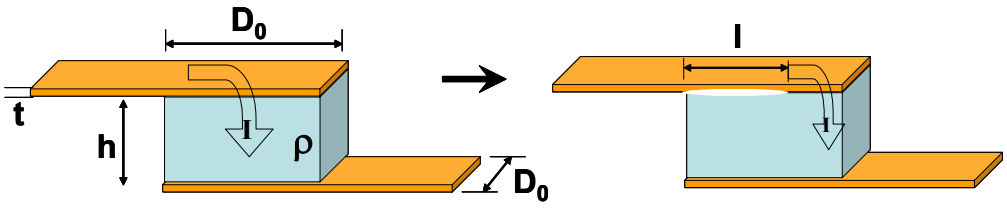
$$R_{block}^{0} = \rho_{solder} \frac{h}{D_0 \times D_0} \tag{4.2}$$

With a bump height of ~70μm, R^0_{block} is 2~3mΩ. When an interfacial crack, with length l, propagates along the interconnect/solder interface, the contact area between the solder block and the interconnect is reduced to $(D_0\text{-}l)\times D_0$. Also, the current has to run through extra distance l in the interconnect before it reaches the solder. Therefore, the resistance change is,

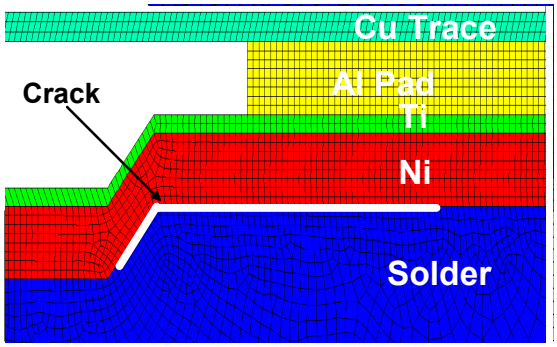
$$\Delta R_{total} = \Delta R_{block} + \Delta R_{interconnect} = \frac{l}{D_0 - l} R_{block}^{0} + \rho_{Cu} \frac{l}{D_0 \times t} \tag{4.3}$$

The FEA model is shown in Figure 4.16(b). Cracks with varying lengths were inserted at the interface of the solder and the UBM. The model was then

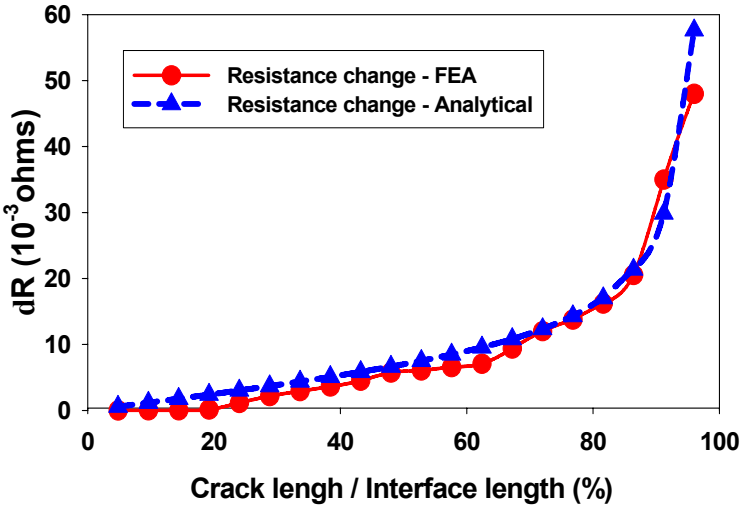
applied with a constant current and the voltage drop across the solder was calculated. The resistance was determined by Ohm's law.



(a)



(b)



(c)

Figure 4.16 The correlation between EM induced crack propagation and the resistance change in the solder bump

The resistance change with respect to the crack length (in terms percentage of the entire interface) was calculated and shown in Figure 4.16(c). One can see that the resistance change is less than 50mΩ until the crack is over 95% of the total interface area.

A typical V_g trace from EM test is shown in Figure 4.17. The Vg trace can be divided into three distinct stages. In stage I, V_g increased from 0 to ~30mV. In this stage, V_g increased smoothly, corresponding to the void incubation and growth period discussed in section 4.4. At the end of this stage, V_g increased to over 30mV, equivalent to a sharp resistance change of over 60mΩ. From Figure 4.15, a resistance change of this magnitude suggests some kind of structural damage such as voids or cracks which had dominated the solder/UBM interface. In stage II, V_g fluctuates abruptly, indicating the recovery and re-generation of the defects. Finally, a V_g increased to over several hundred milli-ohms accompanied by the drop of the current, indicating an electrical open circuit failure had occurred. The time when stage I ended (V_g =30mV) was taken as the failure time of the test structure since that was when the evolutionary EM damage progress was completed. However, tens of milli-ohms change may not be large enough to cause the circuit to fail. Therefore, the time when open failure occurred (V_g =300mV) was also taken for comparison.

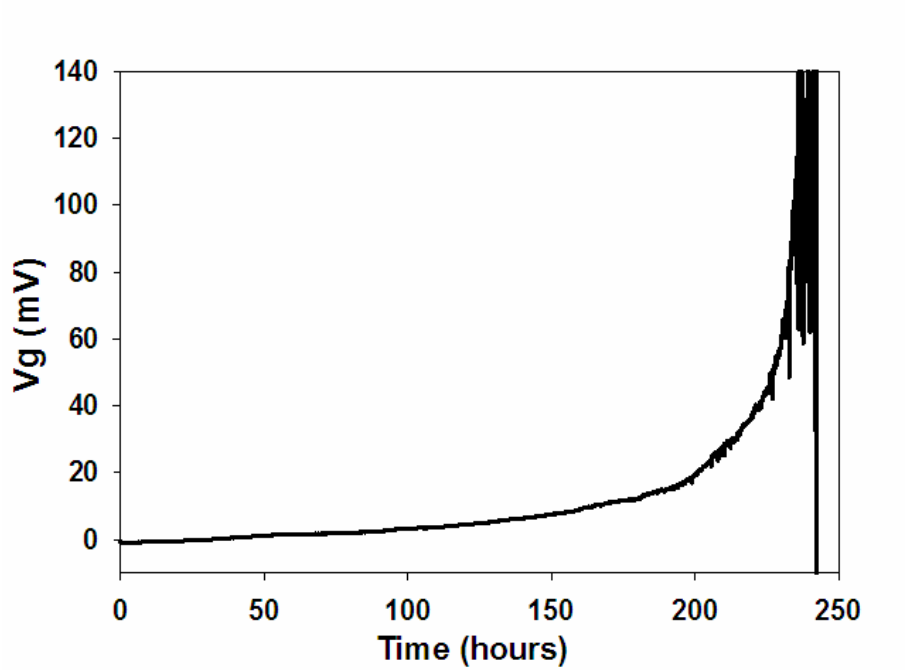


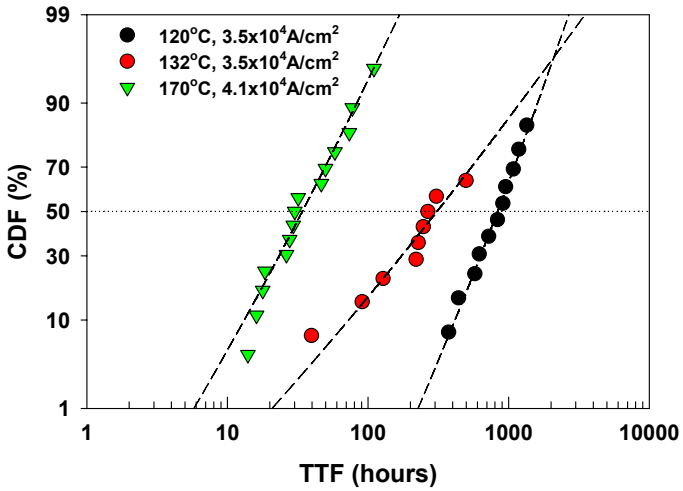
Figure 4.17 Typical V_g traces (Ni UBM 110°C)

4.6.2 Lifetime Statistics

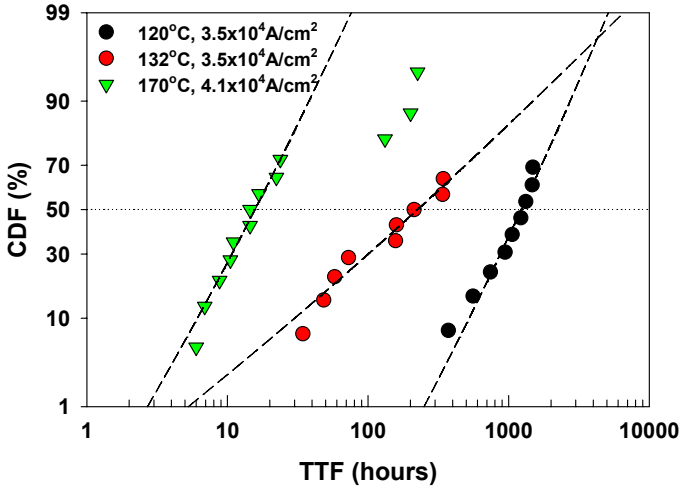
4.6.2.1 Statistical Distribution of the EM Lifetime

The time when 50% of the samples had failed also known as the mean-time-to-failure (MTTF, t_{50}) was used as the characteristic EM lifetime. The log-normal cumulative distribution function of failure (CDF) of the 2-link test structures using V_g =30mV and V_g =300mV failure criteria are summarized in Figure 4.18 and 4.19. Most of the data fits the log-normal curve well, except the

data from samples with Ni UBM tested at 132 and 170°C using a V_g =30mV criteria.

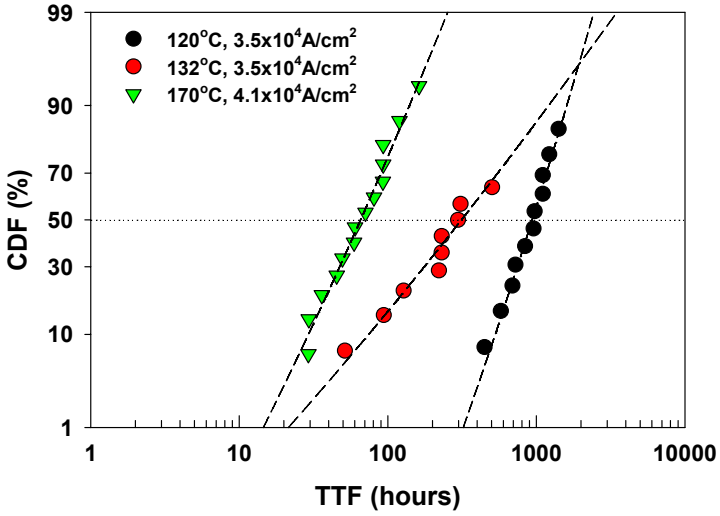


(a)

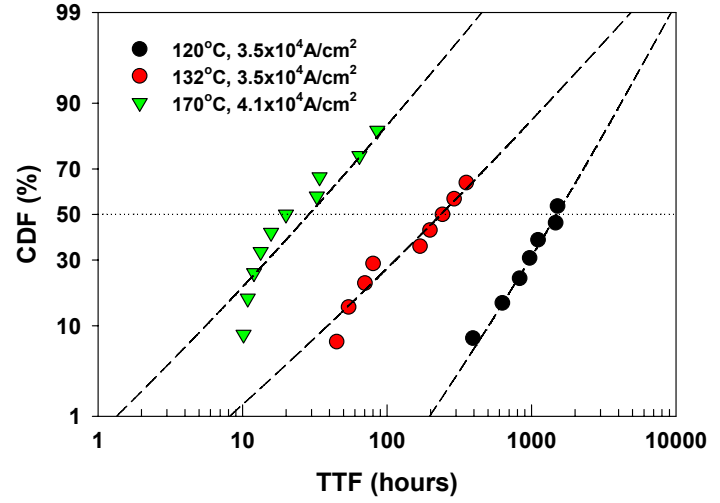


(b)

Figure 4.18 Temperature dependence of electromigration lifetime statistics of solder bumps (N=2) with (a) Cu and (b) Ni UBM based on a V_g =30mV failure criterion



(a)



(b)

Figure 4.19 Temperature dependence of electromigration lifetime statistics of solder bumps (N=2) with (a) Cu and (b) Ni UBM based on V_g=300mV failure criterion

For samples with Ni UBM tested at 132 and 170°C (V_g =30mV criterion), there were two groups of failures in each of them with one showing shorter lifetime than the other. It was suspected that a bimodal EM failure might exist in this case. Bimodal failure has been used to describe the extrinsic early failures in the Cu interconnect electromigration tests [4.5-4.8]. As shown in Figure 4.20, the bimodal distribution has two log-normal probability density functions, pdf^{ex} and pdf^{in}. The superscripts denote the failure modes, extrinsic and intrinsic. Each of them has its own t_{50} and σ (t_{50}^{ex} and t_{50}^{in}; σ^{ex} and σ^{in}). The failure in the extrinsic mode is normally induced by process defects that facilitate the EM damage evolution. Therefore, t_{50}^{ex} is normally much smaller than t_{50}^{in} and the extrinsic failure mode is also called the *early failure*. The total probability density function is:

$$pdf = xpdf^{ex} + (1-x)\,pdf^{in} \tag{4.4}$$

where x is the proportion of the extrinsic failure mode. The cumulative failure distribution can then be written as:

$$cfd = \int pdf = x\int pdf^{ex} + (1-x)\int pdf^{in} = xcfd^{ex} + (1-x)cfd^{in} \tag{4.4}$$

Usually, the proportion of the early failures is quite small, only a few percent of the population since this mode is ‘abnormal’. In this study, however, the ‘early failed’ samples formed over 50% of the population. For that reason, we would rather call it ‘alternative failure mode’. The data was then fitted with bi-

lognormal distribution as shown in Figure 4.21. A similar trend existed in Cu samples but was not as evident as in the Ni samples.

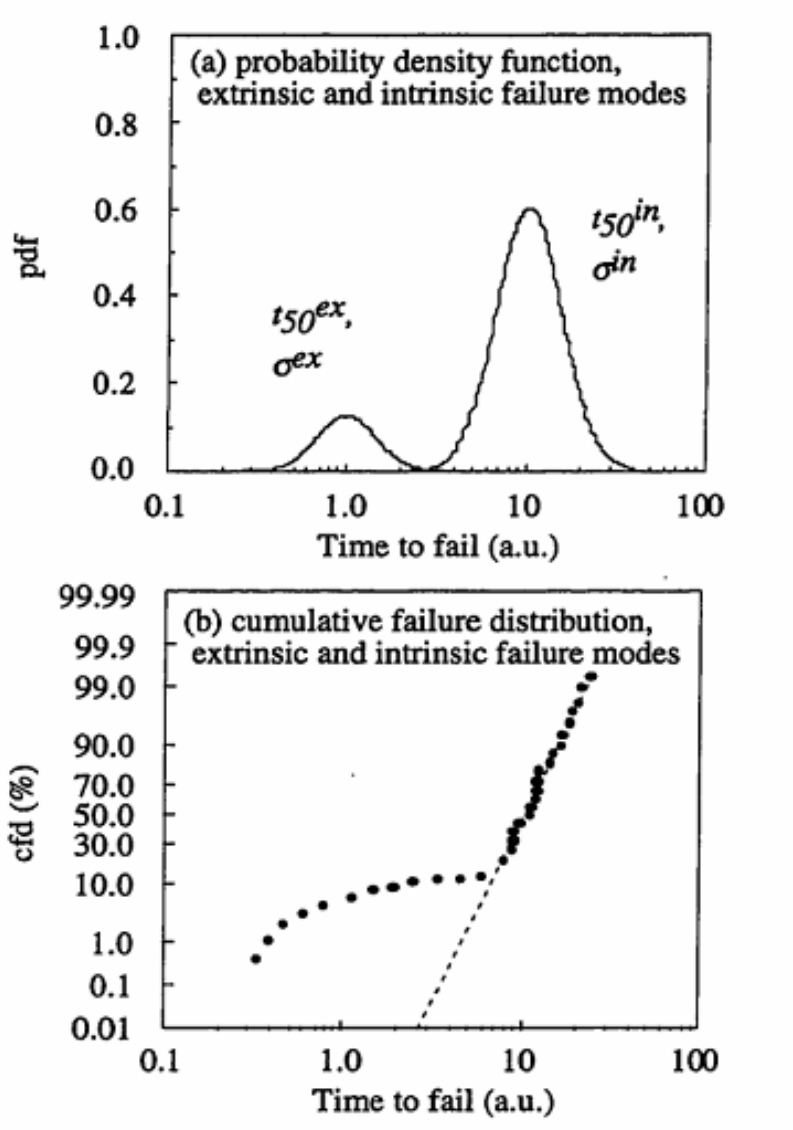


Figure 4.20 (a) Example of a bimodal probability density function (b) The cumulative failure distribution [4.7]

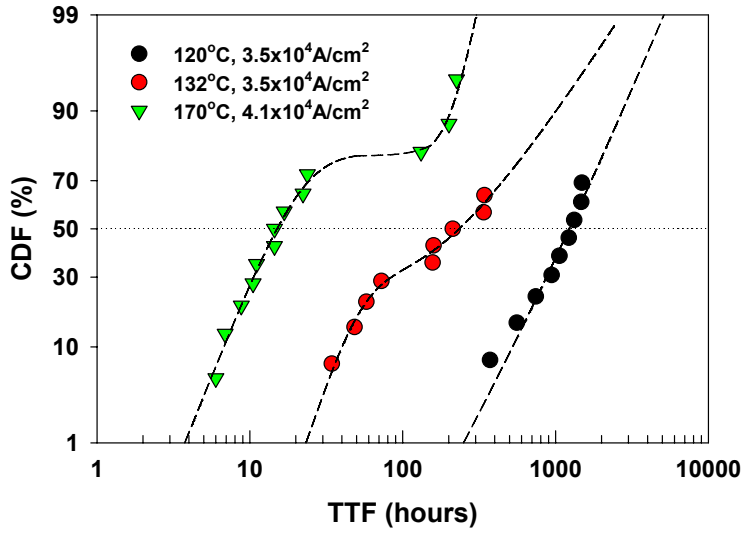


Figure 4.21 EM lifetime statistics of Ni UBM samples with bi-lognormal distribution

Since the samples has 2-link structures, deconvolution was done based on the weakest link approximation to yield the MTTF of single solder bumps. The deconvolution results for Figure 4.18 and 4.21 are listed in Table 4.3 and 4.4.

Table 4.3 EM lifetime statistics of Pb-free solder bumps with Cu and Ni UBM based on two kinds of failure criteria at various test conditions

Solder Bump Temperature (^oC)	Current Density j ($10^4 A/cm^2$)	Failure Criterion							
		Vg=30mV				Vg=300mV			
		Cu UBM		Ni UBM		Cu UBM		Ni UBM	
		t_{50}	σ	t_{50}	σ	t_{50}	σ	t_{50}	σ
120	3.5	1181	0.64	1879	0.78	1247	0.52	2577	1
132	3.5	634	1.32	583	1.66	643	1.32	613	1.84
170	4.1	54.8	0.87	25.1	0.87	98.1	0.74	65.5	1.51

Table 4.4 EM lifetime statistics of Pb-free solder bumps with Ni UBM with bimodal failure

Solder Bump Temperature (^oC)	Current Density j ($10^4 A/cm^2$)	Failure Mode 1		Failure Mode 2		Proportion of Mode 1
		t_{50}	σ	t_{50}	σ	
120	3.5	n/a	n/a	1879	0.78	0
132	3.5	47.7	0.36	683	1.15	14%
170	4.1	14.7	0.57	240	0.3	54%

4.6.2.2 Temperature Dependency of the EM Lifetime

The result for the temperature dependence of t_{50} for both Cu and Ni UBM samples is plotted in Figure 4.22. To determine the activation energy of the EM process, the data was fitted using *Black's equation*:

$$t_{50} = Aj^{-n}e^{\frac{Q}{kT}} \tag{4.5}$$

where Q is the activation energy in eV, j is the current density in the solder bump in A/cm^2, k is the Boltzmann's constant, T is the bump temperature, A is a constant that must be determined experimentally and n is the current dependency coefficient. Electromigration studies on interconnects has shown that n is between 1~2 [4.9-4.12]. Due to the limited number of samples and time, not enough tests were performed to determine the value of n. Therefore, activation energy was determined assuming the upper and lower boundaries, n=1 and n=2. For samples with Cu UBM, Q=0.84~ 0.89eV when n varies from 1 to 2; for samples with Ni UBM the range is 1.1~1.2eV. Further EM studies need to be carried out as a function of current density in order to determine the value of n.

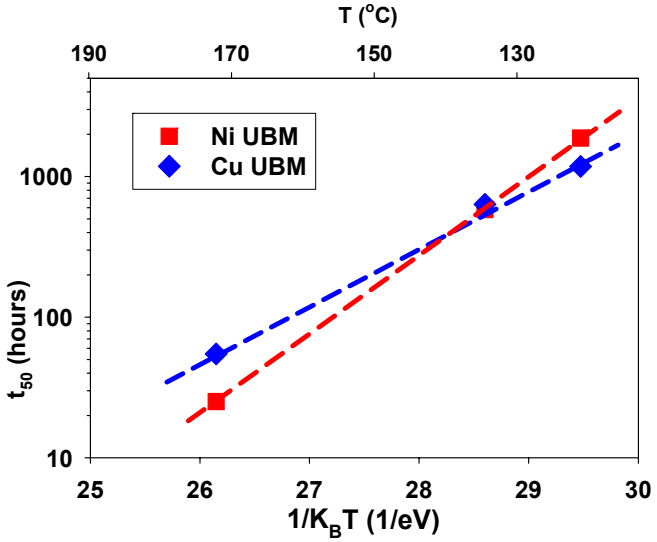


Figure 4.22 Temperature dependence of EM lifetime

4.6.2.3 Standard Deviation of the Test

The standard deviation of t_{50} ranged from 0.64~1.66, higher than the average value for chip-level interconnects (~0.3). The standard deviation is an important parameter when extrapolating the lifetime data to a different level of failure rate. For example, instead of t_{50}, the more commonly used characteristic lifetime in the semiconductor industry is $t_{0.01}$, which means the time when the first device out of ten thousand devices failed. The relationship between t_{50} and $t_{0.01}$ is:

$$t_{0.01} = t_{50} e^{-3.719\sigma} \tag{4.6}$$

The larger the σ, the smaller $t_{0.01}$ will be obtained for the same t_{50}. $t_{0.01}$ reduces from 33% to only ~0.2% of t_{50} when σ increases from 0.3 to 1.66.

The standard deviation in failure times comes from different sources. Some sources are better understood and can be eliminated or at least estimated. In this study, one major source is the temperature variation amongst the samples. For interconnect EM tests, the test current is relatively low, in the range of 1mA, and heat dissipation of the order of milli-watts. The Joule heating-induced temperature difference between samples is about 1°C with little convection in the atmosphere. In this test, precaution has been made to keep the sample temperatures as close to each other as possible. All the samples were kept in a convection oven with forced air circulation and the die side was clamped to a massive copper plate. However, the temperature variations between samples still reached about 3~5°C due to the large current (~1A) and heat dissipation (several Watts). The σ induced by the temperature difference can be estimated as:

$$\sigma = \frac{Q}{k}\left(\frac{1}{T} - \frac{1}{T + \Delta T}\right) \tag{4.7}$$

where Q is the activation energy in eV, k is the Boltzmann's constant, T is the test temperature and ΔT is the maximum temperature difference between samples. Figure 4.23 illustrates the change of σ with test temperature and the temperature difference between samples. It is estimated that the σ induced by temperature differences is 0.29~0.38 in this study.

The failure mode change with temperature revealed by the study also affects the standard deviation. The standard deviations at different bump temperatures are shown in Figure 4.24. One can see that σ at 132°C bump

temperature is much higher (1.32~1.66) than the other two temperatures (0.64~0.87). For samples with Ni UBM, it is clear from Figure 4.21 and Table 4.3 that the failure mode dominating at higher temperature (Failure Mode 1) began to show its effects at 132°C (~14% of all the failures). The difference between the lifetimes of the two failure modes expanded the lifetime distribution. Similar analysis can be done for Cu UBM samples.

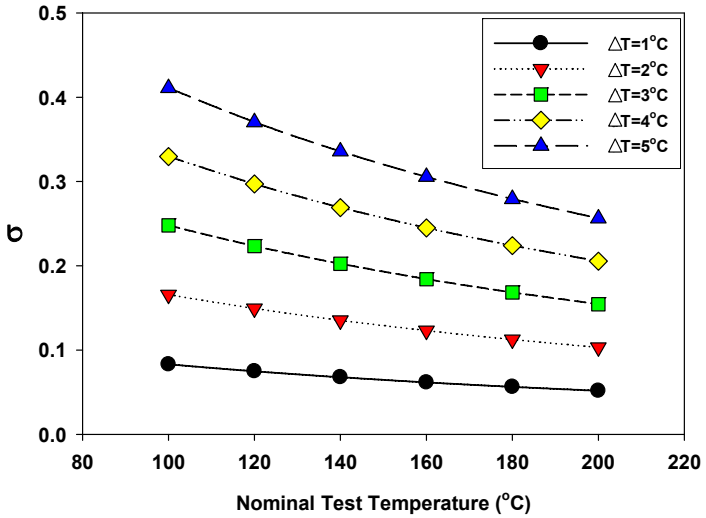


Figure 4.23 Standard deviation estimation under different test temperature

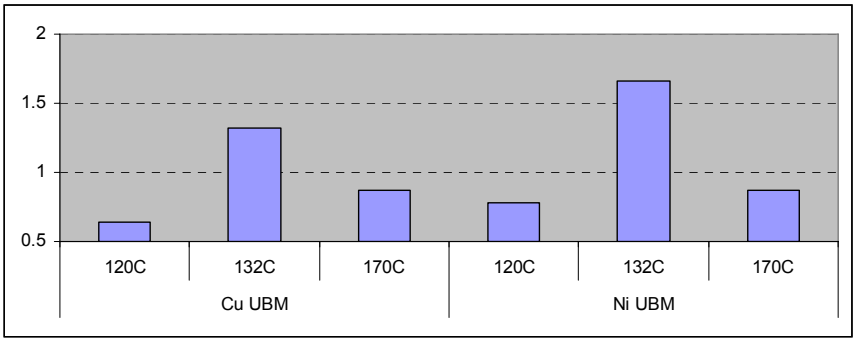


Figure 4.24 Standard deviation (σ) at different temperature

4.6.2.4 The Effect of Failure Modes

Although Black's equation was used to fit the lifetime data and nominal activation energies were obtained, the validity of Black's equation in the solder bump EM test needs to be examined more carefully. As described in 4.4, the failure modes of Cu and Ni bump could change with temperature. Consequently, different models are considered necessary for different failure modes.

High Temperature failure: In the EM test at 120^{o}C ambient temperature, the failure was induced by the de-wetting of the solder from the UBM after the Cu or Ni layer was completed consumed. Therefore, the EM lifetime equals to the time needed for the growth of the intermetallic compound to consume the entire Cu or Ni layer:

$$MTTF_{EM} \approx t_{IMC\_Growth} \tag{4.8}$$

and

$$Q_{EM} \approx Q_{IMC} \tag{4.9}$$

where $MTTF_{EM}$ is the mean-time-to-failure of the EM test, t_{IMC_Growth} is the time from the IMC growth to consume the entire Cu or Ni layer, Q_{EM} is the activation energy for the EM test and Q_{IMC} is the activation energy of the IMC growth. For Cu/Sn diffusion couples, the activation energy of IMC growth has been found to be 0.63~1.14eV [4.13-4.16]. For Ni/Sn diffusion couples, the activation energy is 0.52~1.33 [4.13, 4.17-4.19]. From (2.15), under electron current, the IMC growth

is proportional to the current density applied. Therefore, the current density factor n in Black's equation is equal to 1.

Low Temperature failure: In the EM tests at 90°C ambient temperature, the failure process involved voids nucleation and propagation along the solder/UBM interface. Therefore, the EM lifetime equals to the incubation time of the void nucleation, t_{inc}, and the time for the void to propagate through the entire interface, t_{growth}:

$$MTTF_{EM} = t_{inc} + t_{growth} \tag{4.10}$$

$$MTTF_{EM} = \frac{A_{inc}}{j^{n1}} e^{\frac{Qinc}{kT}} + \frac{A_{growth}}{j^{n2}} e^{\frac{Qgrowth}{kT}} \tag{4.11}$$

where for the incubation and void growth process respectively, Q_{inc} and Q_{growth} are the activation energies; *n1* and *n2* are the current density exponents; A_{inc} and A_{growth} are proportionality constants. From the analysis in chapter two,

$$t_{growth} = \frac{l_{\text{int}erface}}{v_{growth}} \tag{4.12}$$

where $l_{interface}$ is the length of the solder/UBM interface and v_{growth} is the growth rate of the void along the interface. Recall (2.15), $v_{growth} \propto j$, so

$$t_{growth} \propto j^{-1} \Rightarrow n2 = 1 \tag{4.13}$$

For the incubation time, no rigorous analysis has been done to theoretically investigate the current density exponent as compared to the work by Kawasaki and Hu [4.20] which suggested that n1=2. More detailed experiments are

necessary to examine the activation energies and the current density exponents for the two processes.

As discussed in 4.2.6.3, there seems to be a cross-over temperature around 132^{o}C at which the dominating failure modes changes. Therefore, extreme caution is needed when extrapolating the lifetime data from the accelerated EM lifetime test over the cross-over temperature to normal operating conditions below it.

4.7 SUMMARY

A parametric study was performed on Sn-Ag, Pb-free solder bumps with two types of UBMs. All the open failures were found in anode bumps with electron current flow from die to substrate side. The EM failure mechanism for solder bumps was found to be temperature dependent. At higher temperature, the dominating failure mode was the de-wetting of the solder from the UBM induced by the UBM formation and dissolution. At lower temperature, the open failure was due to the void nucleation and propagation along the solder/UBM interface with little damage to UBM. The nominal activation energies based on Black's equation were found to be ~0.84-0.89eV for Cu UBM and ~1.13-1.21eV for Ni UBM.

Chapter 5: Electromigration Study in High Lead Solder System

Sn-Pb solder with high Pb content (>90 wt% Pb) has been used as the material for C4 bumps ever since the first flip-chip package. High-Pb solder shows good thermal stability and thermal fatigue resistance since the melting point of high Pb solder is over 300^{o}C, far beyond normal application temperature. At the same time, it also has lower Young's modulus and yield strength compared with eutectic Sn-Pb and Pb-free solders which helps reduce the stress level in the die level interconnects. Therefore, high-Pb solder is still the most commonly used C4 bump material in flip-chip packages. The electromigration study of flip-chip packages with high-Pb solder bumps from two different manufacturers will be reported in this chapter.

5.1 EM STUDY ON FLIP-CHIP PACKAGE FROM MANUFACTURER I

5.1.1 Experimental Details

The flip-chip package from manufacturer I was a high performance central processing unit (CPU). The 11x11mm die was attached to a ceramic (alumina) substrate. The bumps were formed with high-Pb solder (97wt%Pb-3wt%Sn). The solder bump, as shown in Figure 5.1, was 110 μm in diameter. The under-bump metallization (UBM) structure is Cu/(Cu,Cr)/TiW on the die side with 60μm passivation opening. The substrate side metallization layer was Ni.

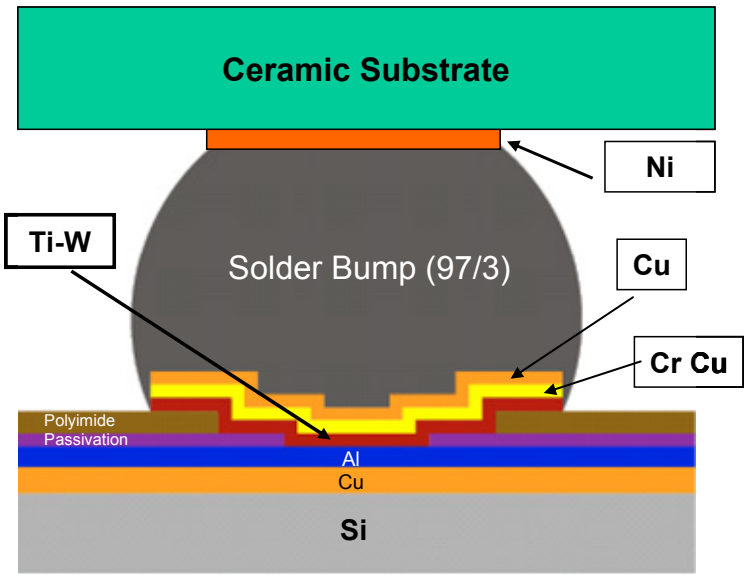


Figure 5.1 Illustration of the solder bump structure from Manufacturer I

For each package, a pair of solder bumps was selected to perform EM tests, as shown in Figure 5.2. The two solder bumps were connected to each other by a Cu layer on the die side. Each bump was connected to individual pins on the ceramic pin grid array substrate, and then to the cathode or anode of the power supply, respectively. After assembly, the gap between the die and the substrate was underfilled. As shown in Figure 5.2, starting from the cathode of power supply, the electron current passed from the substrate through the bump on the cathode side (the cathode bump), and into the Cu layer on the die side. It then passed through the bump on the anode side (the anode bump), back to the substrate, and returned to the power supply.

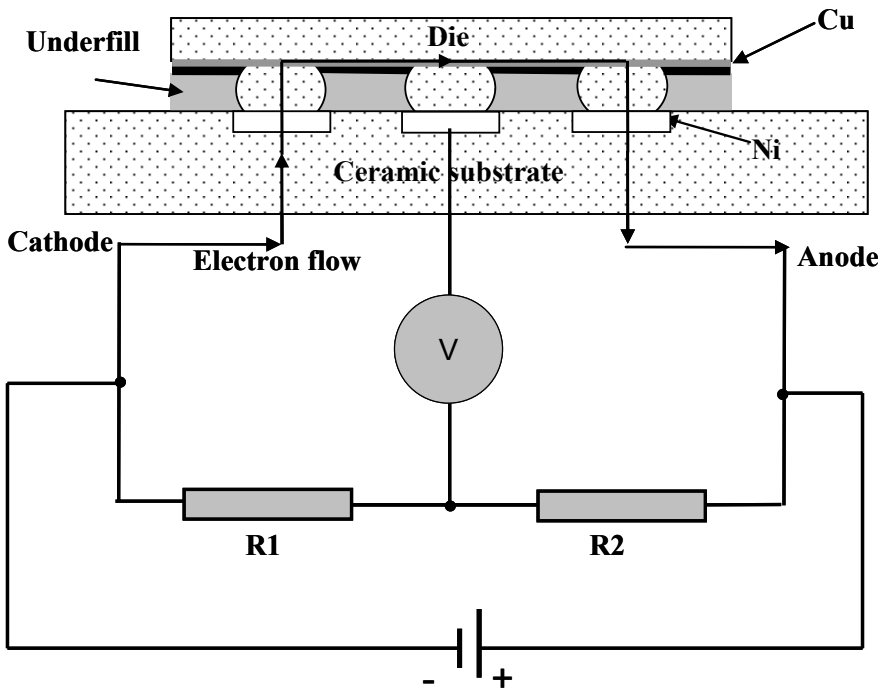


Figure 5.2 Cross-section of solder bump pair under test and test circuitry

The current applied to each sample was 1.0 amp. The current density was then calculated to be $1.1 \times 10^4 A/cm^2$ if the current was averaged by the maximum cross-sectional area of the solder bump or $3.5 \times 10^4 A/cm^2$ if averaged by the cross-sectional area of the passivation opening. EM tests were performed at four different ambient temperatures. The Joule heating effect induced by the large current was calibrated by attaching thermocouples to the top of the die and verified using the finite element analysis. The results are listed in Table 5.1. Unless specified, all the temperatures mentioned in the rest of the section will be the solder bump temperature.

Table 5.1 Temperature measurement results of the EM test

Ambient (Oven) (^{o}C)	136	155	172	184
Die Top (^{o}C)	165	185	207	215
Solder Bump (^{o}C)	172	191	214	221

To determine whether the electromigration phenomenon in solder was dominated by the direction of electron current, 4 extra samples were stressed using 0.25Hz square wave AC current with 1 amp amplitude at 214^{o}C. The positive and negative current had the same duration in one cycle of the square wave as shown in Figure 5.3. Because of the low frequency applied, the AC current performed similarly to DC current in terms of Joule heating generation and temperature distribution inside the test structure. The only difference is that AC showed no polarity of the current when averaged for a long time.

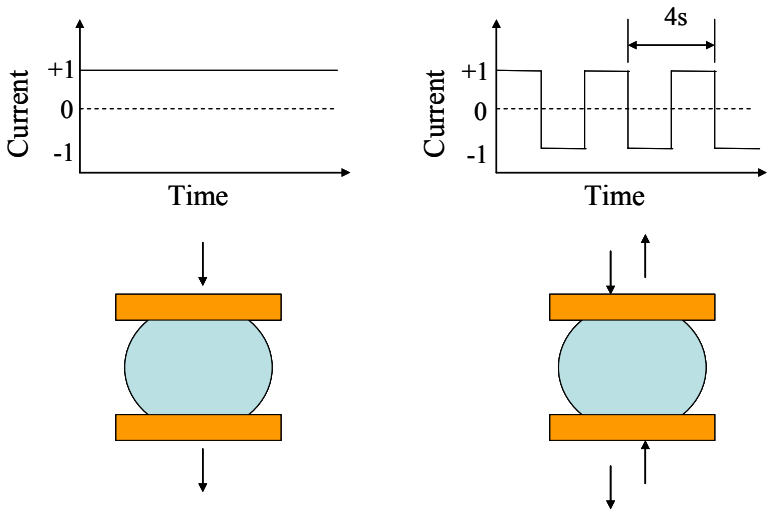


Figure 5.3 Current stressing: DC vs AC

After electromigration testing, selected packages were cross-sectioned and polished to the mid-plane of the tested bumps for failure analysis. Scanning electron microscopy (SEM) was employed to examine the morphology of the bumps, and energy-dispersive x-ray spectroscopy (EDS) was used to detect the elemental distribution in the solder bumps.

5.1.2 Solder Resistance Trace during EM Test and Failure Criteria

Figure 5.4 shows a typical trace of the off-balance voltage, V_g, monitored over a period of 600 hours taken from one EM test at 191^{o}C. From the trace, one can see that V_g continues to increase. From circuit analysis, the increase of V_g corresponds to a resistance increase in the anode bump that is induced by the EM damage. Among all the test samples, electromigration failure was observed only

in the anode solder bumps where the electron current passed from the under bump metallization (UBM) to the substrate side.

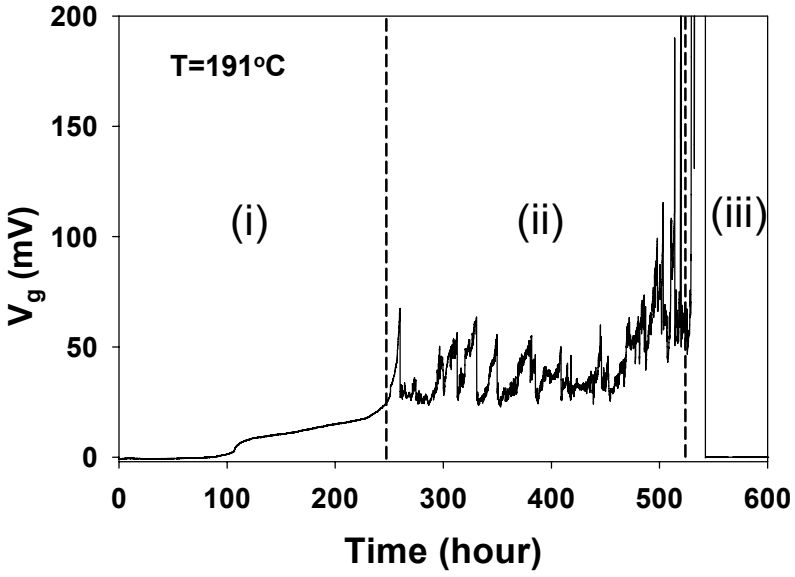


Figure 5.4 Typical off-balance voltage V_g versus time in EM test

As showed in Figure 5.4, the V_g trace can be divided into three distinct stages. In stage I, V_g increased smoothly, indicating a slow and gentle period of resistance increase in the anode bump. At the end of this stage, a small spike appeared, corresponding to a sharp resistance change of ~30-100mΩ. According to the analysis in chapter 4, a resistance change of this magnitude suggests that an electromigration-induced void/crack has grown to almost the entire length of the interface. In stage II, V_g fluctuated abruptly, indicating the development and recover of the EM damage. Finally, at the beginning of the stage III, there was a large off-balance voltage increase after 530 hours, indicating an electrical open

circuit failure of the anode solder bump. We took the time where the resistance of the anode bump increased by ~30mΩ (or the end of the first stage) to be the failure criterion.

As a comparison, Figure 5.5 shows the V_g trace of a sample stressed with AC current at 214°C. One can see that the change of V_g was hardly observable throughout a period of 200 hours. All the 4 samples stressed with AC current performed similarly. At the same time, all the 11 samples with DC current at the same temperature failed within 150 hours. Finite element analysis showed that the temperature gradient across the bump is ~300-400°C/cm. This suggests that, compared with electromigration, the thermo-migration induced damage at such thermal gradient level [5.1, 5.2] does not play a major role in causing solder bump failure when a large current is present.

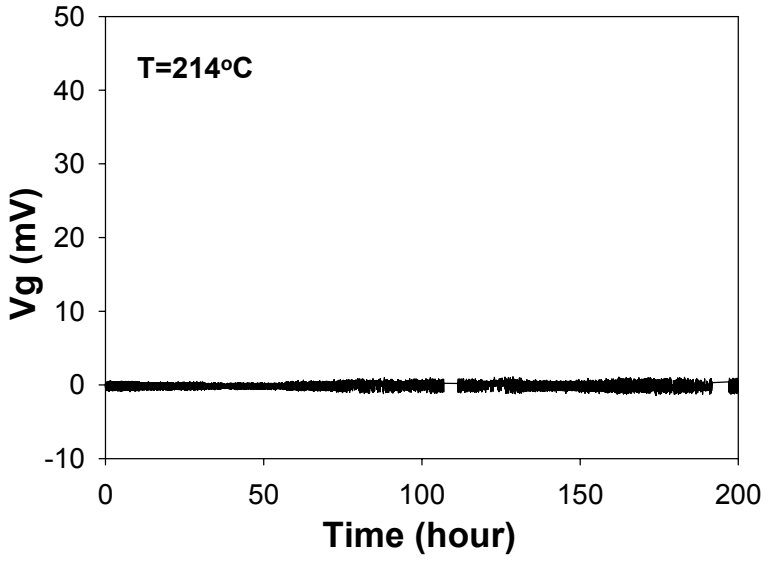


Figure 5.5 Typical V_g trace from EM test with AC stressing at 214°C

5.1.3 EM Lifetime Statistics

Figure 5.6 and 5.7 show the log-normal fitting of the cumulative distribution of failure (CDF) of the EM tests based on 30mV and 300mV failure criteria. The mean-time-to-failure (MTTF) was taken as the time when 50% samples had failed and the lifetime data are shown in Table 5.2. The test temperature has a strong effect on the solder bump EM lifetime. As temperature increases from 172^{o}C to 191^{o}C, the MTTF reduced 73%, from 1768 to 487 hours. The standard deviation, σ, of the lifetime statistics were consistent with previous solder EM studies, most of which is larger than 0.5.

Table 5.2 EM lifetime statistics of High-Pb solder bumps based on two kinds of failure criteria at various test conditions

Solder Bump Temperature (^{o}C)	Failure Criterion			
	V_g =30mV		V_g =300mV	
	t_{50}	σ	t_{50}	σ
172	1768	1.09	1950	1.18
191	487	0.77	595	0.74
214	172	0.38	220	0.40
221	160	0.88	208	0.86

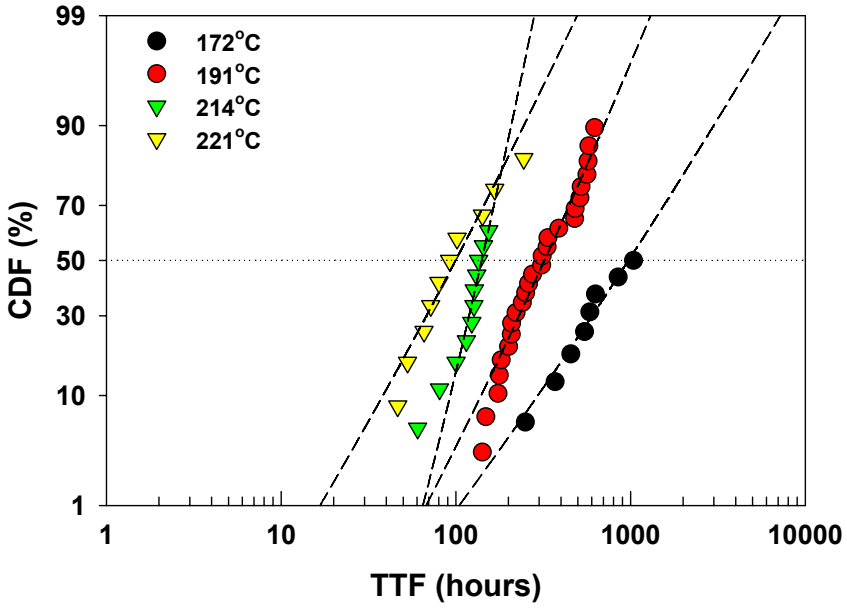


Figure 5.6 Cumulative distribution of failure (V_g =30mV criterion)

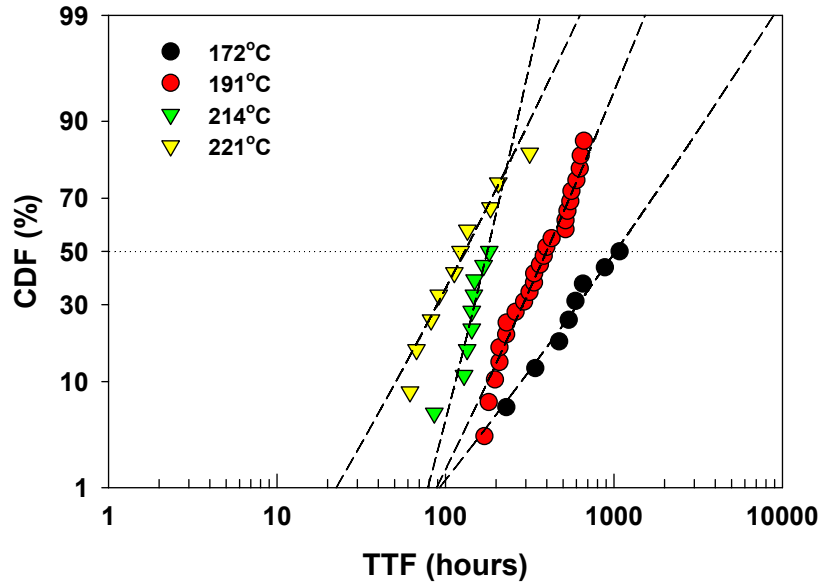


Figure 5.7 Cumulative distribution of failure (V_g=300mV criterion)

Black's equation is used to fit the lifetime-temperature dependence. According to the equation, the lifetime versus 1/kT data was drawn in a semi-log plot and fitted linearly in Figure 5.8. Activation energy of the solder bump EM, Q, was determined from the slope of the line to be 0.91±0.19eV.

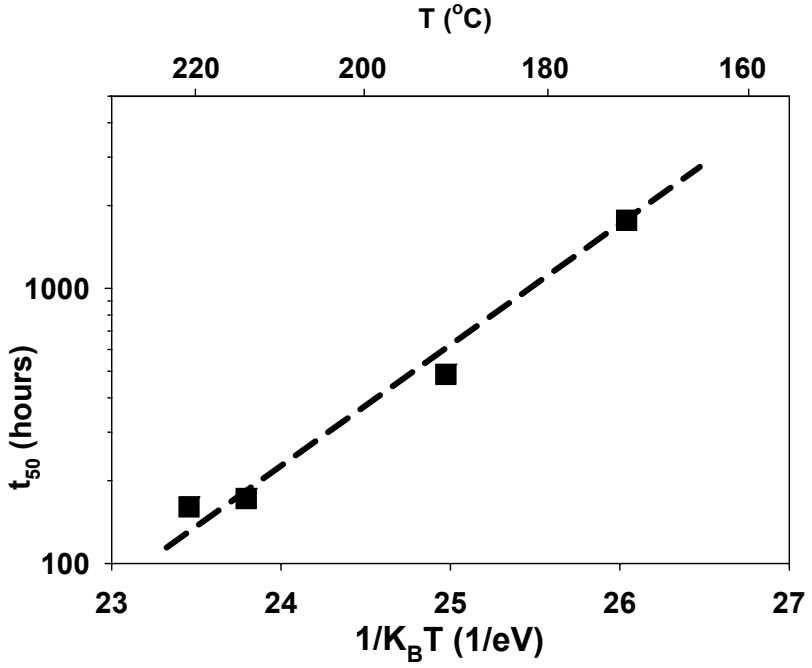


Figure 5.8 Lifetime-temperature dependence of high lead solder electromigration

5.1.4 Failure Analysis

To understand the electromigration mechanism, samples were taken out of the oven at different stages of the test. These samples were then cross sectioned and examined using SEM and EDS. Figure 5.9 shows the EDS element mappings of the anode bump at stage I and III. From Figure 5.9 (a) and (c), one can see that Sn and Cu accumulated in the UBM area in stage I, indicating the formation of Cu-Sn intermetallic compound after reflow. EDS analysis showed that the intermetallic compound was Cu_6Sn_5. With continuing EM test, Sn and Cu atoms migrated away from the original UBM area driven by the electron flow. Finally, most of Sn and Cu moved to the metallization layer on the substrate side, as shown in Figure 5.9 (b) and (d), indicating the dissolution of Cu_6Sn_5 from UBM area. The Cu thin film in UBM and the Cu_6Sn_5 compound acted as the adhesion layer between solder and the UBM. Therefore, the depletion of Cu and Sn induced dewetting of solder from UBM, which finally developed into an open circuit failure in the solder bump. Some research work on eutectic solder [5.3, 5.4] showed that the migration of Pb driven by electron flow may be responsible for solder bump EM failure. It is not likely the case in our study, because the diffusivity of Sn and Cu in Pb is 10^3-10^6 times that of self-diffusion of Pb [5.5]. The electromigration of Cu and Sn would have finished a long time before significant amount of Pb migrated and induced EM damage. The deformation of the anode solder bump after failure is probably due to the softening of solder under high temperature induced by local Joule heating.

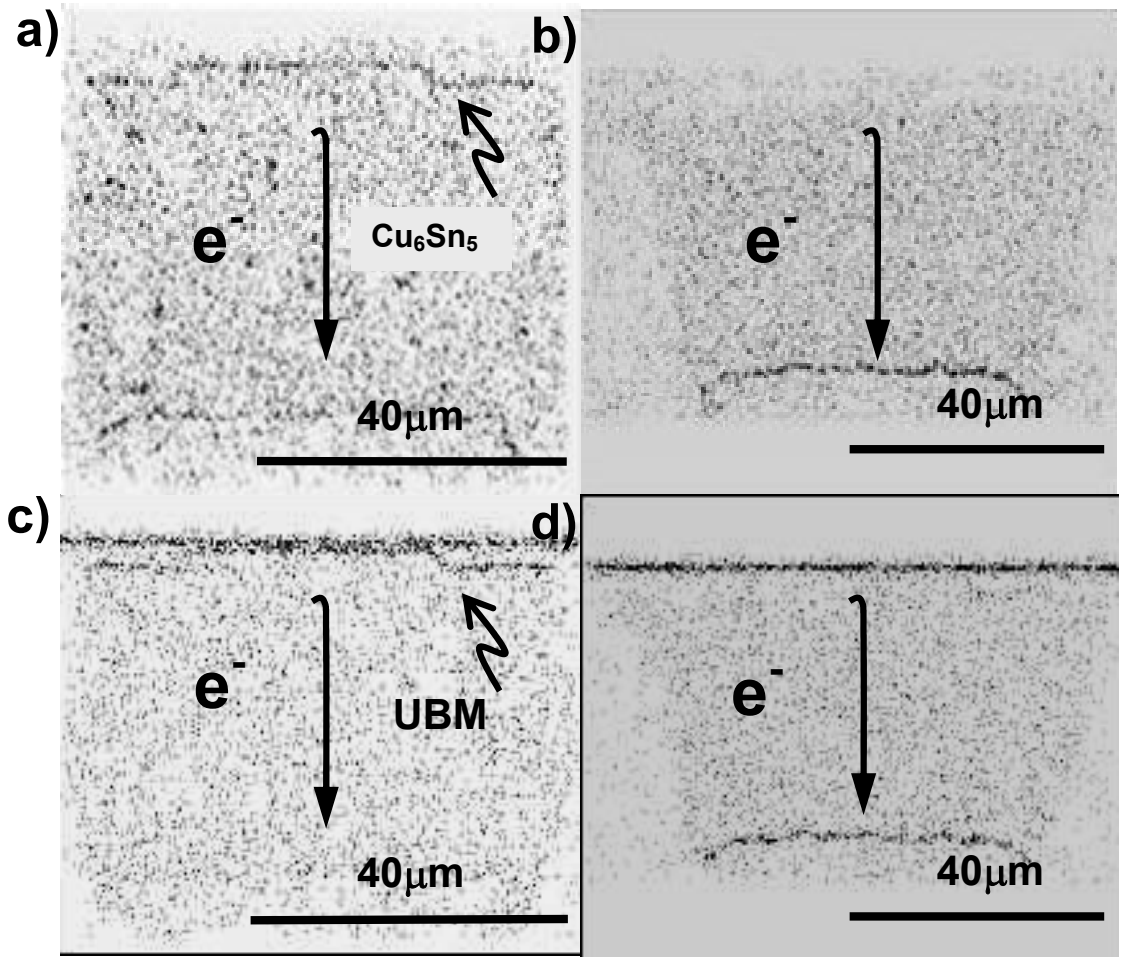
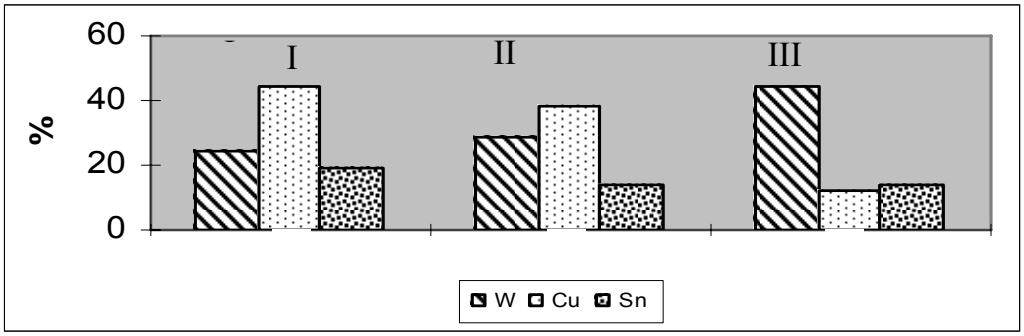


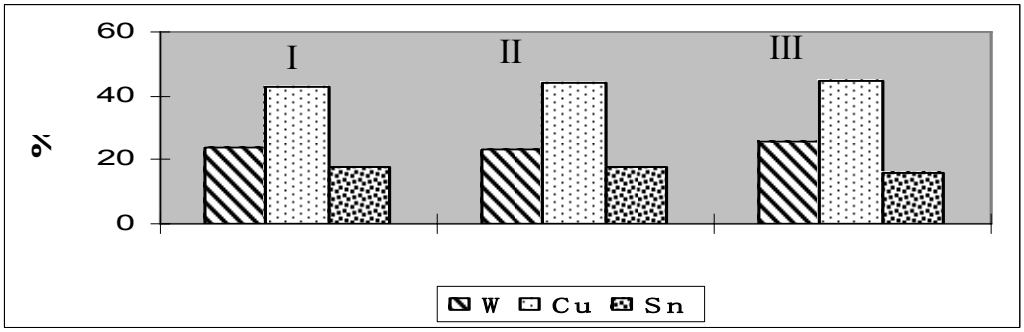
Figure 5.9 Element mappings of anode bump
a) Sn, stage I; b)Sn, stage III; c)Cu, stage I; d)Cu, stage III

EDS compositional analysis of the UBM area is shown in Figure 5.10. Tungsten in the UBM was chosen as an inner standard for element concentration comparison, since it did not migrate under electron flow. From figure 5.10, it is shown that the concentration of Cu and Sn keeps decreasing during the EM test.

In stage (II) and (III), the concentrations of Cu are 71% and 14% of that in stage (I), respectively. For Sn, the values are 61% and 40%. For the cathode solder bump, EDS analysis showed that Cu and Sn remained in the UBM with the concentrations unchanged.



(a)



(b)

Figure 5.10 EDS compositional analysis of W, Cu, Sn

The SEM images of a pair of solder bumps from the final stage are shown in Figure 5.11. One can see that the anode bump showed an open failure, as suggested by the V_g trace, while the cathode bump remained almost intact. The failure site in the anode bump is at the die/solder interface. As stated before, the migration of Pb is not the major failure mechanism. The deformation of the anode

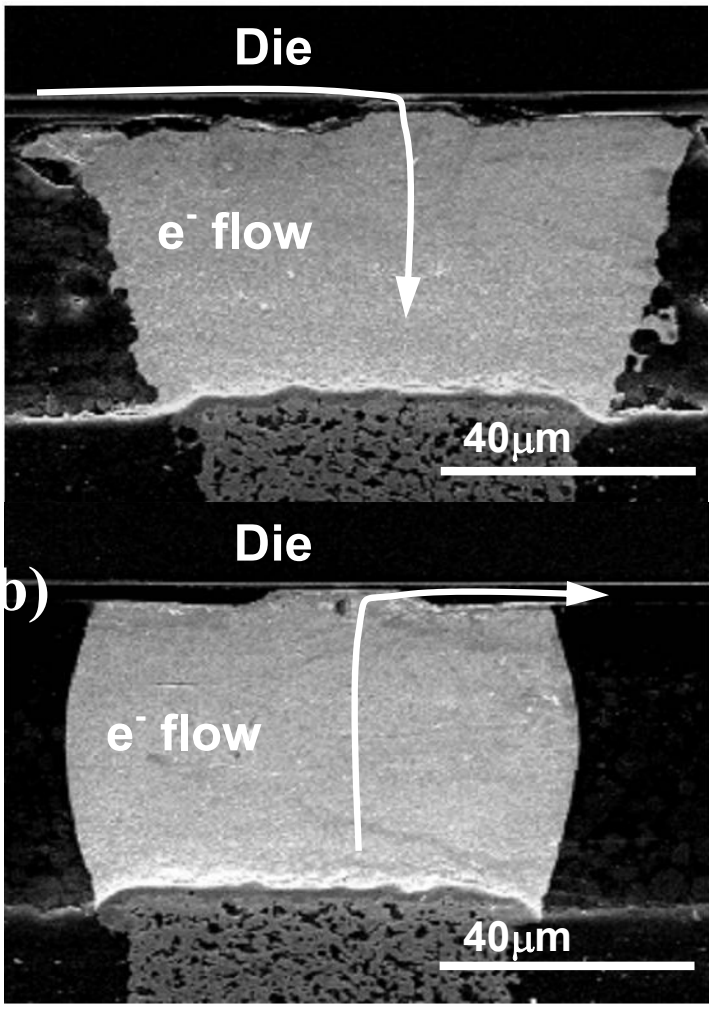


Figure 5.11 SEM image of the cross-section of the solder bump pair from the final stage (T=191°C) a) anode bump b) cathode bump

solder bump after failure is probably due to the softening of solder under high temperature induced by local Joule heating.

For a bettering understanding of the EM damage evolution, SEM images of one corner of the anode solder bump from different stages of EM test are shown in Figure 5.12. In stage (I), driven by electron current, Cu and Sn migrated toward the substrate side. There were two processes related to the migration of Cu and Sn. One is the formation of Cu_6Sn_5 IMC. Because Cu was the faster diffusing species in IMC[5.6], Cu driven from UBM entered the solder bump and form Cu_6Sn_5. The interface between IMC and solder became rough, as shown in figure 9(a). Because the volume of Cu_6Sn_5 is ~20% smaller than that of the mixture of Cu and Sn atoms, the IMC formation induced a tensile stress along the UBM/solder interface. At the same time, voids migrated against the electron flow direction, and condensed at the UBM/solder interface, forming small cracks. Under a tensile stress, cracks will propagate along the interface. The crack propagation reduced the contact area of the solder bump, increasing the resistance.

The other process is the dissolution of Cu_6Sn_5. The electron flow would disassociate Cu_6Sn_5, and drive Cu and Sn separately away from UBM. The dissolution of Cu_6Sn_5 reduced the interfacial adhesion between the UBM and solder and facilitated the crack growth. In stage (I), void accumulation and crack initiation happened at different places of the UBM, the process was well controlled; therefore, the resistance change was smooth as a function of time.

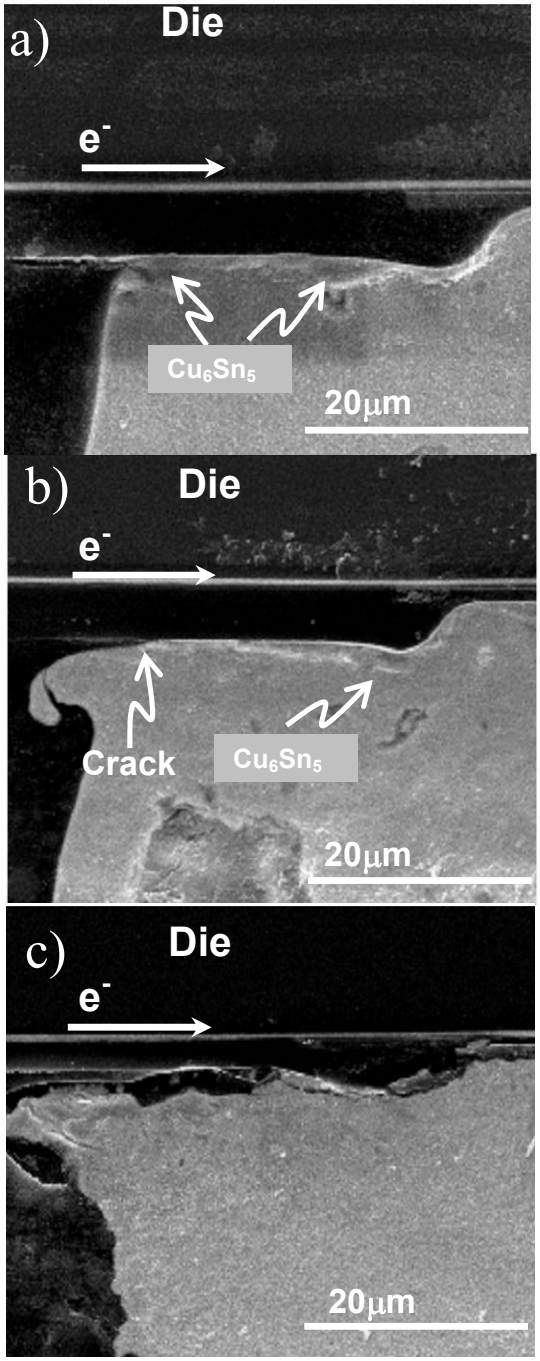


Figure 5.12 The cross-section of the anode solder bumps (T=191^{o}C)

a) stage I, b) stage II, c) stage III

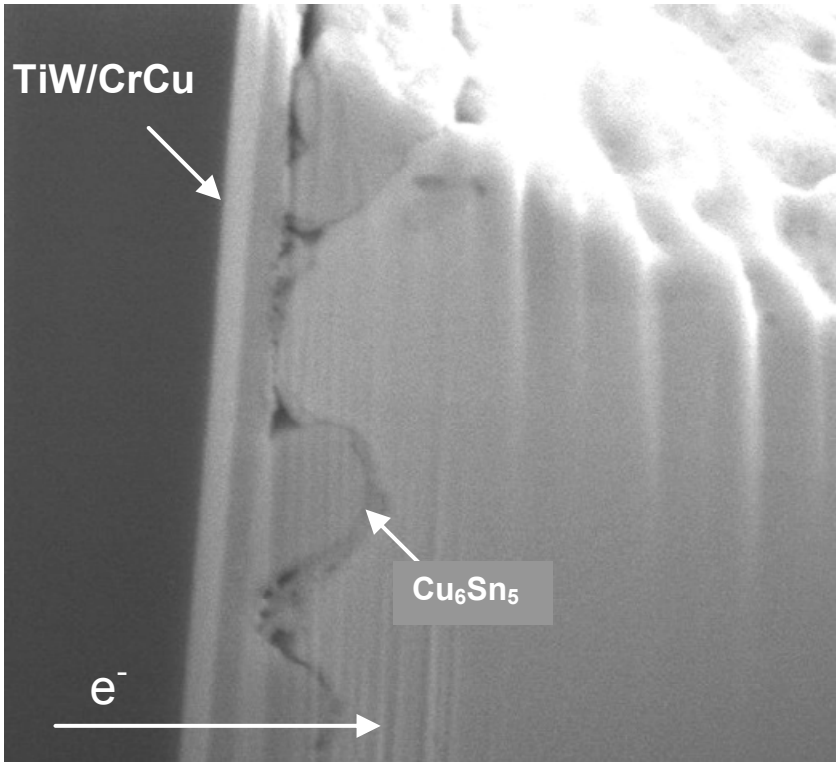


Figure 5.13 The UBM/solder interface of the anode solder bumps at stage II

After a certain amount of time, the crack length reaches such a critical value that it initiates unstable growth. The fast growth of crack reduces the contact area of the UBM/solder interface significantly, resulting in a sudden increase of resistance. From this point, the solder EM process enters stage (II). From the SEM image, Figure 5.12(b), the thinner and incomplete Cu_6Sn_5 layer at the UBM/solder interface confirms the dissolution of the Cu_6Sn_5 IMC. At the interface where Cu_6Sn_5 was hardly visible, cracks exist. From the V_g trace, we can see that resistance of the anode solder bump fluctuated at a much greater level

than in stage (I). This can be explained by Figure 5.13, the SEM image of the area around UBM of the anode bump in stage (II). In some sections of the UBM/solder interface, Cu_6Sn_5 have dissolved completely and cracks propagated along the interface, while there were still some Cu_6Sn_5 left at other sections. Because the bonding between Cu_6Sn_5 and UBM is strong and Cu_6Sn_5 is very hard, when the crack hits a Cu_6Sn_5 particle, it can neither penetrate the particle nor peel it off. It has to go around the particle. This stop-and-go action caused the resistance to fluctuate abruptly. When a Cu_6Sn_5 particle was hit by the crack, it was the only contact area that allowed current to pass, causing serious current crowding and accelerated the dissolution of Cu_6Sn_5.

In the final stage, crack had grown to the full length of the interface, causing an open circuit failure, as shown in Figure 5.12(c). For the solder bump at the cathode side, no morphology changes can be observed, as can be seen in Figure 5.11(b).

5.2 EM STUDY ON FLIP-CHIP PACKAGE FROM MANUFACTURER II

5.2.1 Experimental Details

Flip chip packages from manufacturer II are also with ceramic (alumina) substrates. The high-Pb solder bumps used have a composition of $Sn_{10}Pb_{90}$. There are two different Cu UBM stacks tested and are listed in Table 1. One UBM is electroplated with a thickness of 18μm, while the other is evaporated with a thickness of 2μm. A schematic view of the structures of the packages is shown in

Figure 5.14. Details of the on-chip metallization and the passivation layers are omitted. The on-chip passivation via opening is 57μm for all of the packages. The

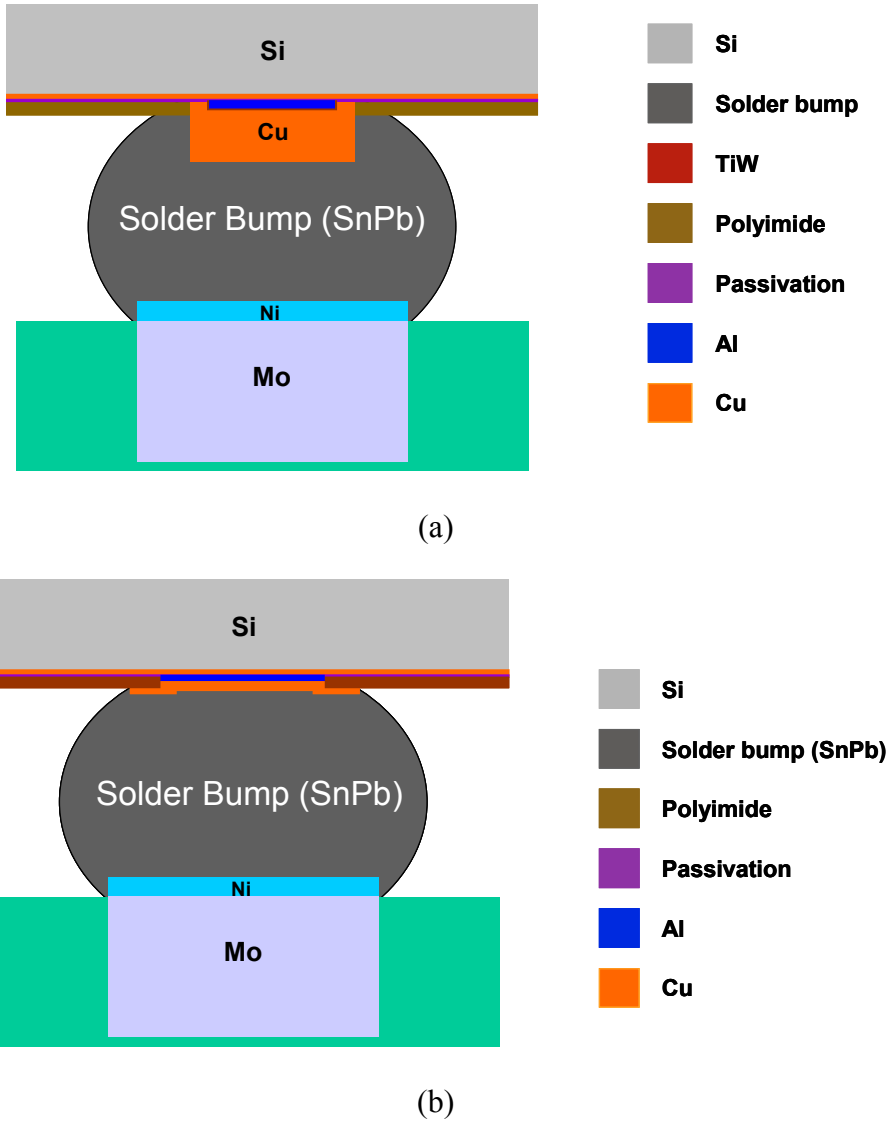


Figure 5.14 Structure of Solder bump: (a) Electroplated Cu UBM (b) Evaporated Cu UBM

diameter of the bumps is about 110μm.

Table 5.3 Configuration of the flip chip packages

Solder material	UBM Deposition	UBM Stack	UBM Thickness (Wetting layer only)
High-Pb	Electroplated	TiW/Cu	18μm
	Evaporated	Cr/CrCu/Cu	2μm

In order to measure the resistance change of solder bumps during the EM tests, a Wheatstone type of circuitry is used (Figure 5.15). One branch of the circuitry contains a fixed resistor, R1, and a potentiometer R2, whose values are in the order of 10^3 ohms. The other branch contains two pairs of solder bumps on the same silicon chip, R3 and R4. At the beginning of the test, the bridge is balanced by adjusting R2, setting the off-balance voltage V_g to be close to zero. During the test, EM damage in the solder bumps will cause the resistance of R3 (or R4) to increase, thus inducing an off-balance voltage V_g. V_g is then used to calculate the resistance change induced by EM damage in the solder bumps. Testing two pairs of bumps in serial doubled the sample size compared to single pair sample test. As shown in Figure 5.15, starting from the cathode of the power supply, the electron flux passes from the substrate through the cathode joint and goes into the Cu layer on the die side. It then passes through the anode joint and

goes into the substrate, and eventually returns to the power supply. Details of the calculation process are discussed in previous chapters.

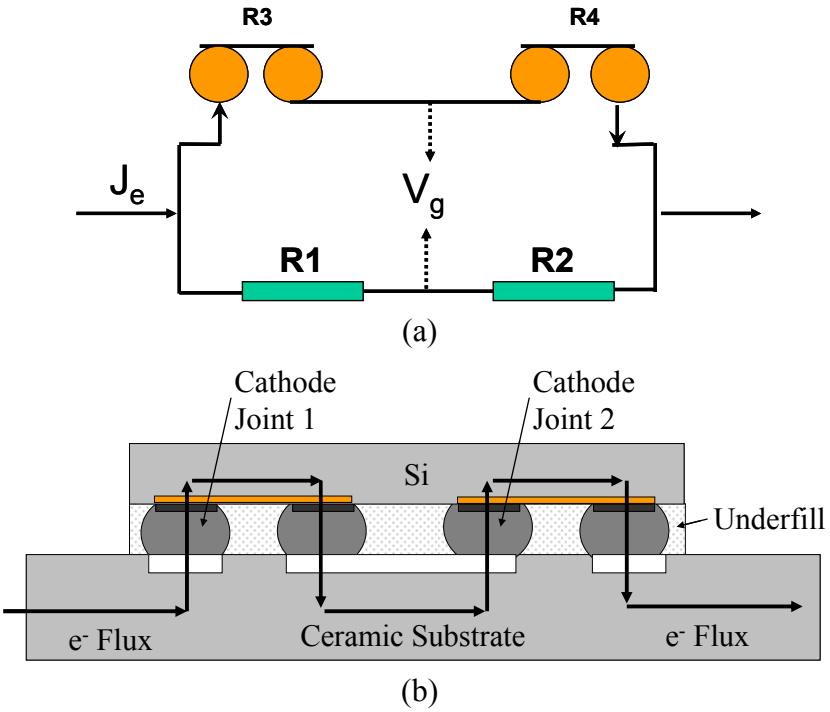


Figure 5.15 The Wheatstone bridge circuitry (a) and a schematic view of the connection of the solder bumps (b)

The test conditions are listed in Table 5.4. Current density is calculated using the area of via opening. At each condition 14 packages of the same type were tested simultaneously in the same oven.

The temperatures are measured with thermocouples that are placed directly on the surface of the silicon chips and then correlated with resistance measurement and FEA simulation. Due to the large amount of the heat generated by the packages during the tests, the set point of the oven is actually much lower than the measured temperature, sometimes up to 40°C.

Table 5.4 Conditions of the electromigration tests

Solder Material	Die Top Temperature (^{o}C)	Temperature (°C)	Current (A)	Current Density (x10^4A/cm^2)
High-Pb	185	195	0.85	3.5
	205	215	1.0	4.1

5.2.2 Results and Discussion

The time to failure (TTF) data of high-Pb solder bumps seem to follow the log-normal distribution as shown by the cumulative distribution of failure (CDF) in Figure 5.16 and 5.17. There is little difference in the distribution whether the 30mV or the 300mV criteria is used. This indicates that the recovery process of the bumps from the EM induced damage is not as vigorous as the Pb-free bumps. The mean-time-to-failure (MTTF) data are listed in Table 5.5. It is clear that the solder bumps with the electroplated UBM have much longer MTTF compared with the evaporated solder bumps.

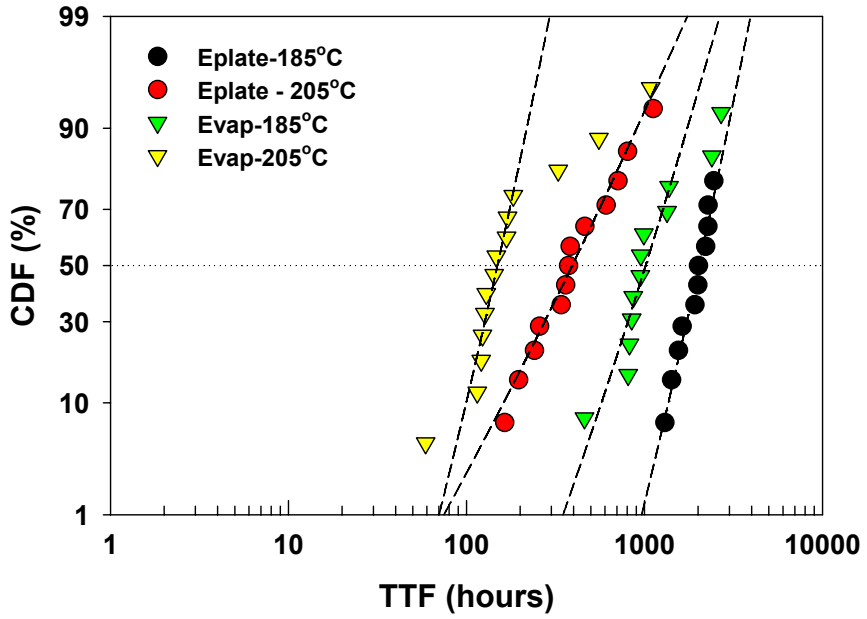


Figure 5.16 Cumulative distribution of failure (V_g =30mV criteria)

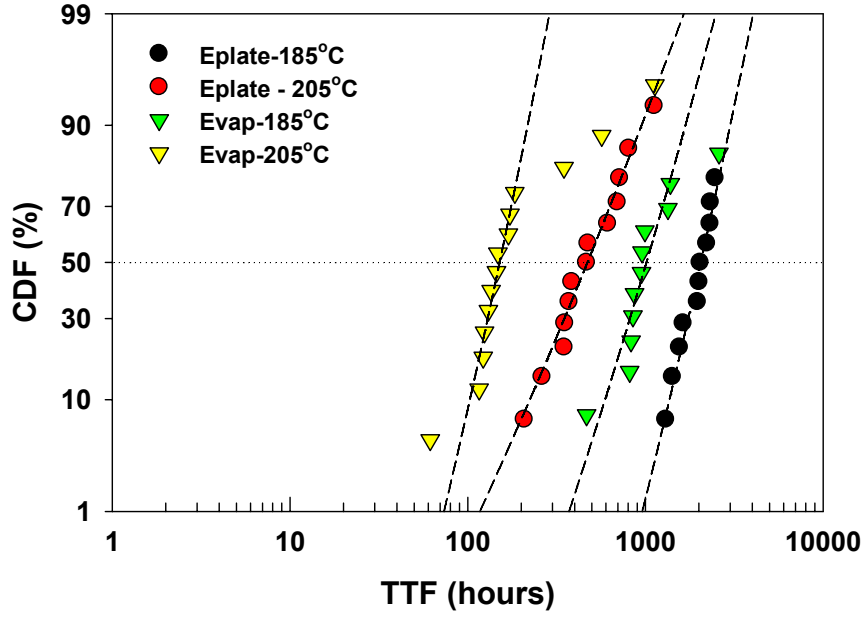


Figure 5.17 Cumulative distribution of failure (V_g =300mV criteria)

Table 5.5 EM lifetime statistics of high-Pb solder bumps based on two kinds of failure criteria at various test conditions

Solder Bump Temperature (^oC)	Current Density (A/cm^2)	Bump Type	Failure Criterion			
			V_g =30mV		V_g =300mV	
			t_{50}	σ	t_{50}	σ
195	$3.5x10^4$	Eplate	2472	0.37	2509	0.37
		Evap	1352	0.52	1327	0.49
215	$4.1x10^4$	Eplate	612	0.82	685	0.67
		Evap	183	0.37	183	0.35

As reported previously, the EM induced damages that cause the open failure in all samples are located within the anode joints, at the UBM/solder interface. Within these joints, significantly increased IMC growth is also observed compared to solder bumps without any electric current during the test.

Shown in Figure 5.18 is a typical cross-section showing the crack that has propagated through the entire interface in an electroplated solder joint. Note the crack is between the remaining Cu layer and the newly formed IMC as discussed in Chapter 4.

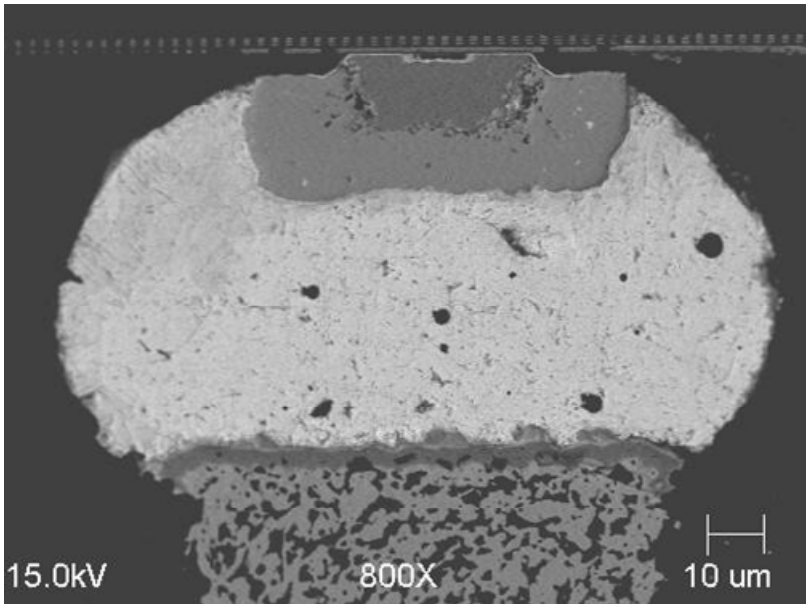


Figure 5.18 Failed electroplated solder bumps

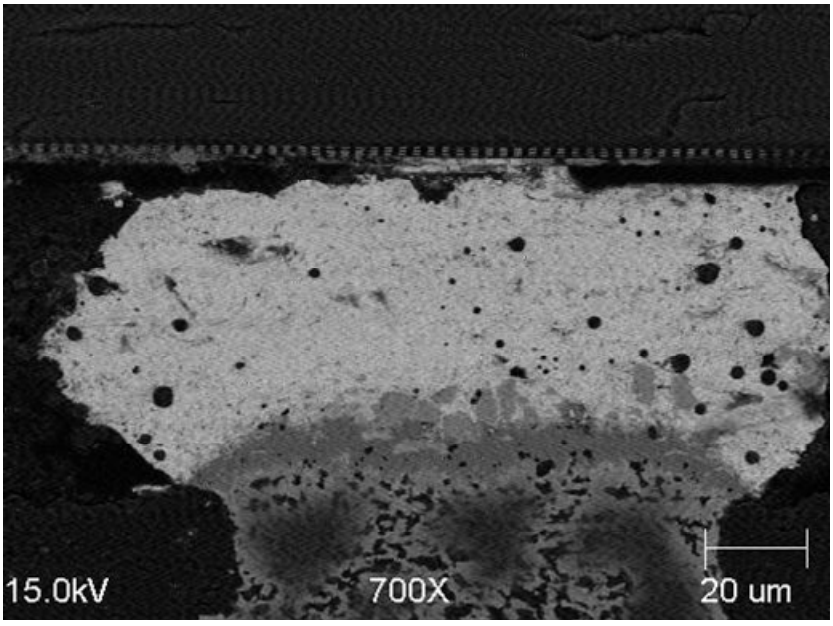


Figure 5.19 Failed evaporated solder bumps

Figure 5.19 shows the cross-section of a failed evaporated solder joint with the thin Cu layer in the UBM. As discussed in section 5.1, the crack is at the joint/silicon interface, and the Cu has completely disappeared from the original location and has been 'pushed' down to the bottom of the joint to form Cu-Ni-Sn IMCs there.

Since the structure of the evaporated UBM sample is very close to that discussed in 5.1 with both of them using high-Pb solder bumps and thin, evaporated Cu-UBM, it would be interesting to compare the performance together. As shown in Figure 5.20, the MTTF of samples from manufacturer II performed better than that of manufacturer I at lower temperature (~195^{o}C). At higher temperature (~215^{o}C), they performed close to each other. Several reasons could have caused the differences in EM lifetime when similar material systems are used. The comprehensive microstructure of the solder bumps and the UBM as well as the assembly process could affect the lifetime of the solder bump by varying the diffusion path through the solder bumps. Another possible reason is the detailed current distribution inside the solder bump. Since the EM induced crack starts from the region with the highest current density, solder bumps with more current concentration would have shorter lifetime compared with those with less current concentration even though their average current density are the same. Since the current concentration is induced by geometry divergence, optimizing the geometrical structure of the solder bump seems to be an effective way to improve EM performance.

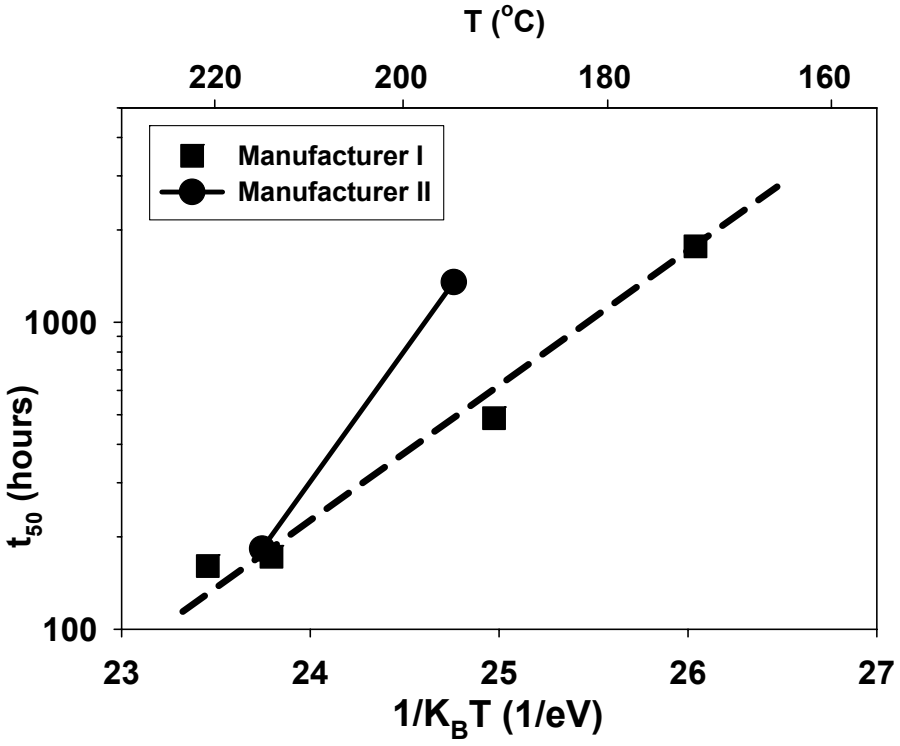


Figure 5.20 Lifetime-temperature dependence of high lead solder electromigration with different manufacturers

5.3 OPTIMIZATION OF CURRENT DISTRIBUTION

In this chapter, finite element analysis will be used to evaluate the effect of geometry on current distribution. Figure 5.21 shows the detailed die side structure of a flip-chip solder bump with Al pad and UBM. In the design process, the parameters flexible to adjustment are the diameter of the bump-to-interconnect via, the diameter of the Al pad, the thickness of the Al pad and the thickness of the UBM. A partial factorial design of experiment was carried out using these four parameters as listed in Table 5.6. The response is the maximum current density seen at the bump-UBM interface.

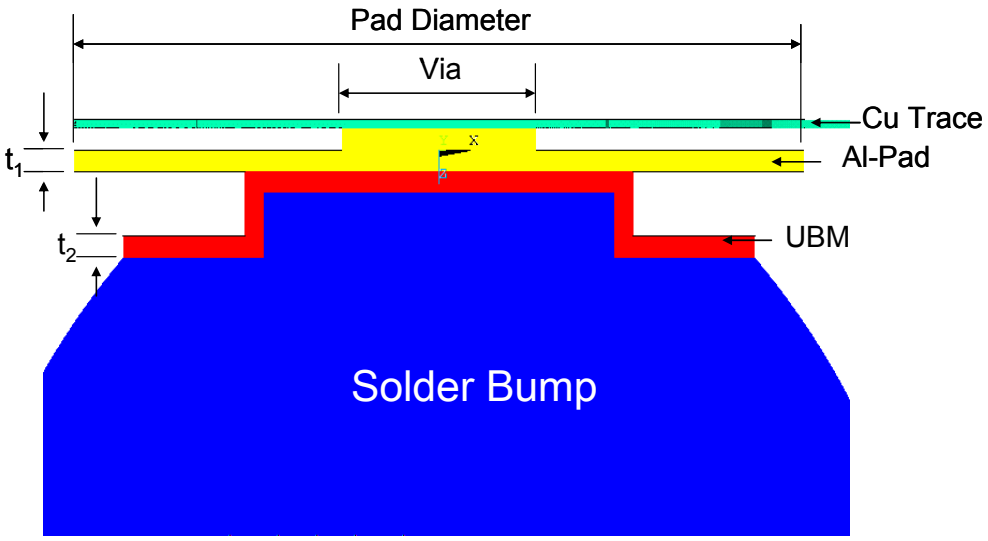


Figure 5.21 Solder bump structure with Al metal pad

Table 5.6 Solder Bump Structure Optimization Design of Experiment

Cell	Via Dia. (μm)	Al Pad Dia (μm)	Al Pad Thickness t1 (μm)	UBM Thickness t2 (μm)	Maximum Current Density (kA/cm^2)
1	20	75	2	2	113.88
2	20	105	2	4	94.83
3	20	75	6	4	70.87
4	20	105	6	2	80.10
5	40	75	2	4	91.02
6	40	105	2	2	115.59
7	40	75	6	2	100.62
8	40	105	6	4	80.34
9	30	90	4	3	85.12

The effectiveness analysis of all the four parameters using Minitab is shown in Figure 5.22. It can be seen that the thickness of the Al pad and the UBM have the monotonic trend on the maximum current density. With larger thickness of both, the maximum current density decreases significantly. The difference can be as high as over 20%. Given that a thicker UBM would take longer time to dissolve, increasing the thickness of the UBM seems to be an effective way to increase EM lifetime than the other parameters. At the same time, the trend of varying the size of the via and the pad is not so clear which means that it is not always beneficial to have larger via which nominally reduces the average current density.

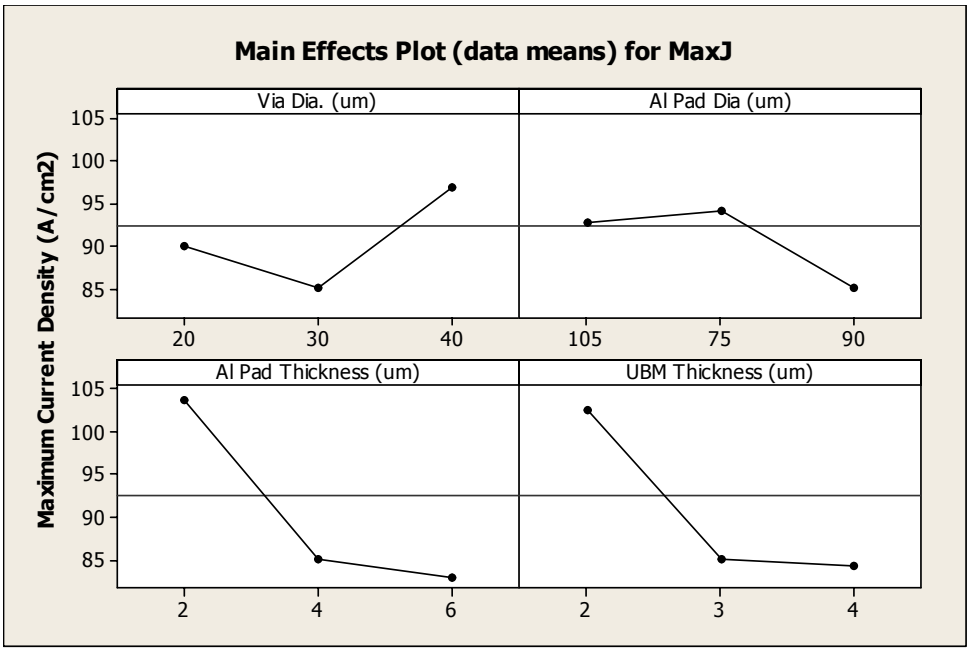


Figure 5.22 Effectiveness analysis of the geometry parameters on maximum current density

A second effort to optimize current distribution is to have a split interconnect trace as shown in Figure 5.23. The idea behind this is that, instead of letting the current 'pour' in to the via from only one side, forcing it to come in from both sides of the via to reduce the highest current density. The simulation results are shown in Figure 5.24. With split interconnects, the current distribution is more uniform and maximum current density reduced ~20%. These design faces some limitation since the design rule does not always allows enough space to have the interconnects split.

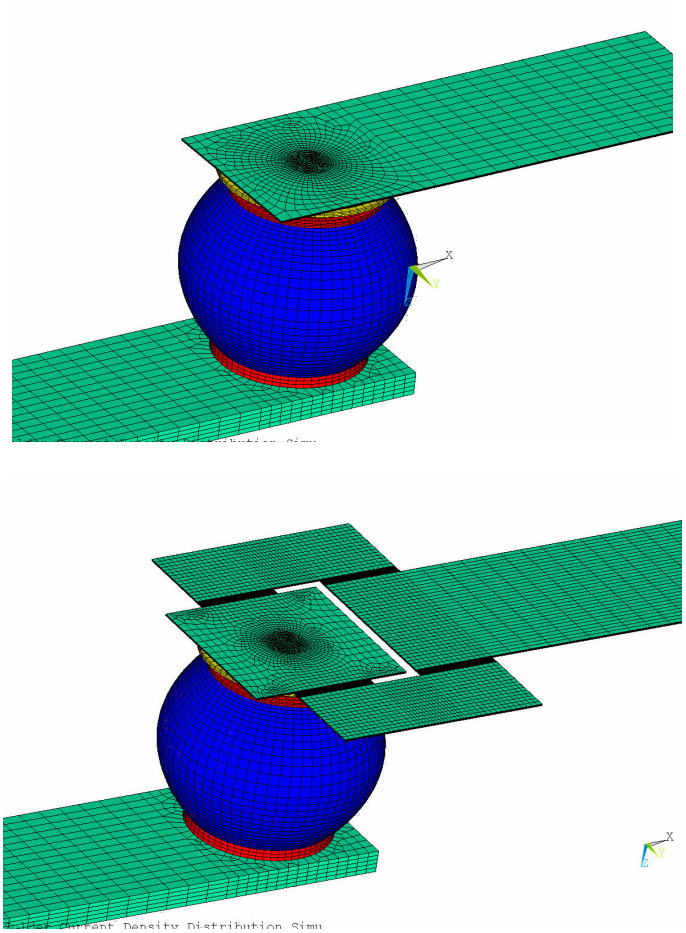


Figure 5.23 FEA model of single and split interconnects

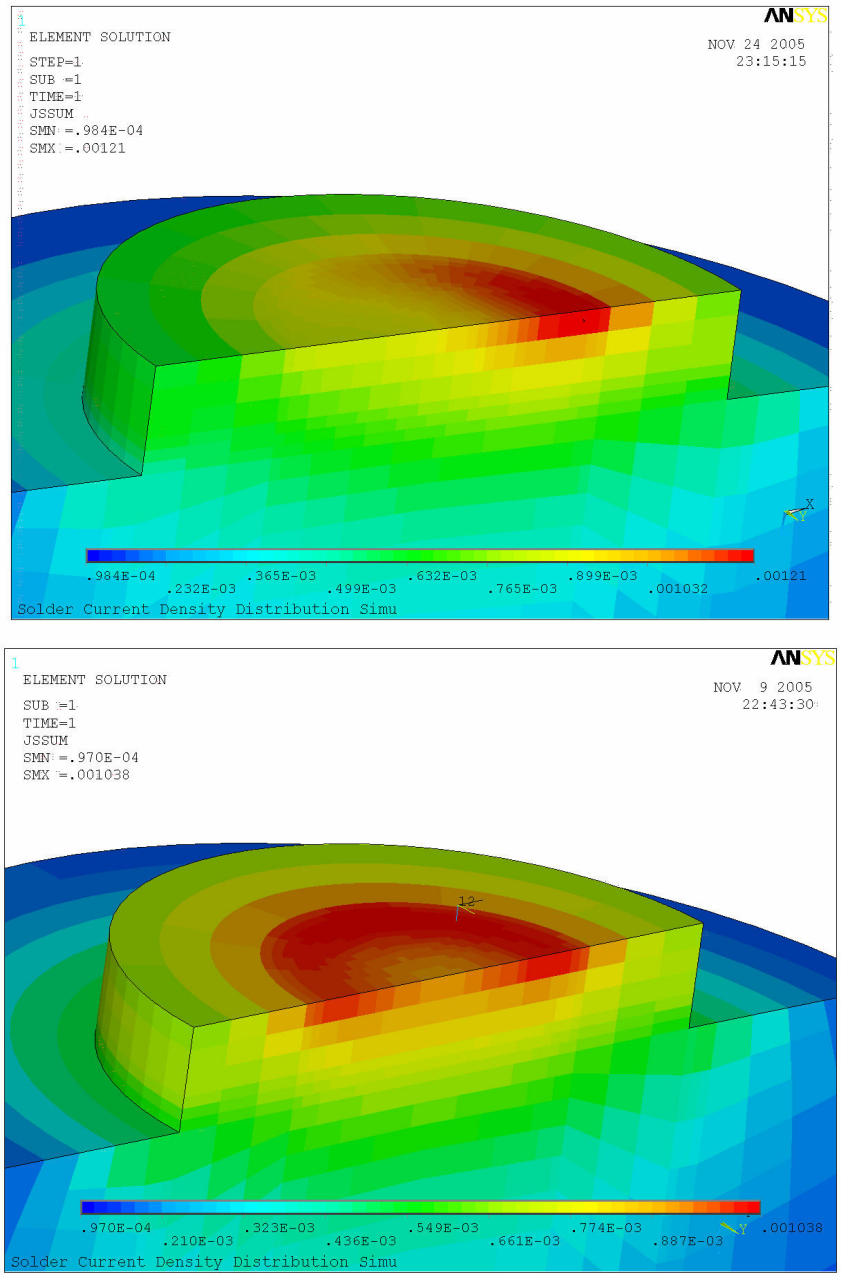


Figure 5.24 Current density distribution in solder bump with single (top) and split interconnects (bottom)

Chapter 6: Conclusions and Future Work

6.1 SUMMARY

This research had three objectives. The first objective was to set up a new and effective experimental technique to examine the damage development and determine the time-to-failure in the electromigration tests since the traditional ohmic resistance method could not provide the necessary sensitivity. The second objective is to examine the failure mechanisms in solder bump electromigration which could be significantly different between different solder bump systems. Pb-free and high-Pb solder alloys with different UBM configurations were studied. The failure mechanisms analysis does not only provide understanding of the root cause but also provide hints to improve the electromigration performance. The third objective is to determine the statistical lifetime of the flip chip solder bumps under electromigration. The outcome provides crucial inputs to set up design rules regarding the maximum allowed working temperature or maximum current density under certain reliability requirement. The lifetime statistics has to be related to the failure mechanisms before they can be extrapolated from experimental conditions to real lifetime conditions.

6.1.1 Experimental System Set up

The test system was constructed based on a high stability current source and a Wheatstone bridge circuit. This configuration ensured that a resistance

change as small as a few milli-ohms that correlated to a partially cracked solder can be detected during the electromigration tests even when large current and thermal noise are present.

Temperature calibration was proved to be important in solder bump electromigration tests. The large current applied through the test structure raised the temperature of the sample above the ambient over tens of degrees. It also created large temperature gradient within the sample itself. Therefore, placing a thermocouple on top of the silicon did not necessarily record accurately the temperature of the solder bump during the test. It was found that the static finite element thermal modeling, calibrated by the thermocouple measurement and resistance analysis, provided more accurate temperature readings of the solder bump structures.

6.1.2 Failure Mechanisms

It was demonstrated that only DC current could induce significantly higher intermetallic compound growth rate and damage accumulation than thermal aging at the same temperature. At the same time, the effect of AC current could be readily reproduced by raising the temperature. This suggested that the electron current was the dominating driving force of the mass transport and induced the damage inside the solder bump as compared to other potential differences such as the temperature gradients.

It was found out that the failure mechanism of the solder bumps in electromigration tests was quite different from that of the chip level interconnects. The EM-induced damages were mostly observed at the solder/UBM interfaces

instead of within the bulk of the solder bump. The most evident mass transport was the migration of the atoms from the UBM layers in the direction of the electron current. This is because:

1. The solder bump structure in the flip chip package is a complex metallurgical system with multiple elements co-existing. The elements come from the solder bump (Sn-Pb or Pb-free) and the UBM layers.
2. For the most commonly used Sn-based and Pb-based solder alloy, the atoms from the UBM layers (Cu and Ni) have much higher diffusivity than the base metal (Sn or Pb) itself. Therefore, the diffusion of Cu and Ni the atoms are much faster under the same electron current.

At the beginning of the electromigration, the intermetallic compound formation at the solder/UBM interface was accelerated. The thickness increased at a significantly faster rate as compared to in thermal aging. With the complete consumption of the UBM layer, the intermetallic compound reached its maximum thickness. After this, the intermetallic compound thickness decreased due to dissolution. The atoms dissolved into the solder bump and diffused to the opposite side along the electron current.

Two major failure modes were found in the solder bump electromigration test. The first mode was the cracking/dewetting induced by the depletion of the UBM layer as described above. The second mode was the cracking induced by EM-enhanced Kirkendall voiding along the interface between different intermetallic layers or the intermetallic layer and the solder.

The damage evolution was found to be non-uniform along the solder/UBM interface. Due to the current crowding effect, the initial void started

at the corner of the via where the maximum current density existed and propagated along the interface. This suggests that an effective way to improve the electromigration performance is to optimize the solder bump/interconnect geometry to have less current crowding and lower maximum current density.

6.1.3 Electromigration Lifetime Statistics

The log-normal distribution was found to be valid in describing the statistical behavior of the solder bump electromigration lifetime. The distribution could be single modal if only one failure mode is dominant and bimodal if two modes were competing with each other. The standard deviation of the log-normal distribution in solder EM test was ~1.0, much higher than that in interconnect EM test (0.3~0.4). The large Joule heating-induced temperature variation was calculated to be accountable for ~30% of the standard deviation. The co-existing failure modes could be another reason for the increased standard deviation. Careful examination is needed to quantify and exclude the 'extrinsic' factors and narrow down the standard deviation to its 'intrinsic' level so that reasonable extrapolation to $t_{0.01}$ could be made from t_{50}.

The temperature dependence of the lifetime was fitted with Black's equation and the activation energy was derived from it. The TTF data of the high-Pb and Pb-free solder joints tested in this study are compared with that of eutectic solder joints from the literature [6.1]. Figure 6.1 is a plot comparing the TTF data at different testing temperatures. Except for the Pb-free solder with Ni UBM, all the samples with Cu-UBM (high-Pb, Pb-free and eutectic SnPb) showed similar

activation energy of ~0.84~0.91. This correlated to the Cu-Sn intermetallic compound growth. The Ni UBM showed slightly higher activation energy of ~1.1eV. At the same test temperature Pb-free solder joints would have much shorter EM life compared with high-Pb solder joints, but longer than eutectic solders.

The UBM material has a strong effect on the TTF. Three UBM structures were tested in the study, electroplated Cu (~18μm), evaporated Cu (~2μm) and the evaporated Ni (~2μm). Depending on the temperature and failure mode, the resistance of the UBMs to EM damage is different. At higher temperature when the depletion of UBM is the dominating failure mode, the thick Cu UBM performs better than the thin Ni UBM. At lower temperature when the Kirkendall voiding induced crack is the failure mode, the Ni UBM has longer lifetime. For Pb-free solder, the transition temperature was found to be 132^{o}C. The ranking of the UBM under different temperatures are,

- Thick Cu> Ni > thin Cu (>132^{o}C)
- Ni>thick Cu>thin Cu (<132^{o}C)

Special attention should be made when extrapolating the lifetime data from high experimental temperature to lower working temperatures because of the switching of failure modes.

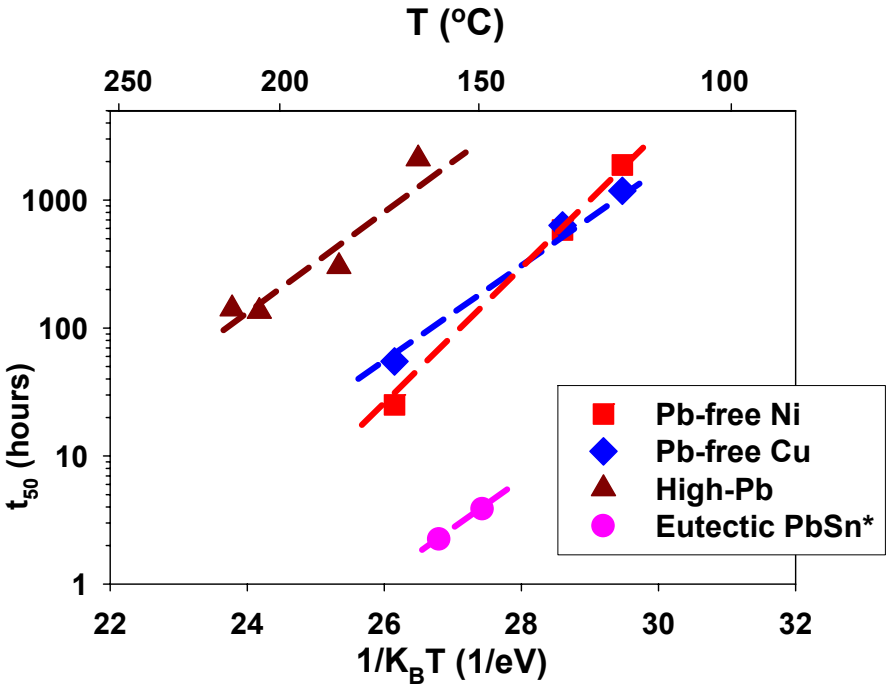


Figure 6.1 EM lifetime comparison between different solder alloys

6.2 SUGGESTIONS TO FUTURE WORK

6.2.1 Improvement in Experimental Technique

Since the determination of the temperature of the test structure is crucial for extrapolating the lifetime data, it would be beneficial to look into new methods to detect the temperature more accurately. As an extension to the method described in chapter 3, extra on-chip temperature sensors (TS) could be placed as close to the test structures (Sa) as possible shown in Figure 6.2. The sensor could be made by routing fine Cu interconnect lines with large resistance. With the

temperature coefficient of the resistor known, the local temperature near the test structure could be recorded by the resistance change. The data could be used either as direct estimation or input to calibrate the FEA thermal models.

Infrared microscopes have also been applied to detect the temperature distribution in the solder bumps during EM tests [6.2-6.4]. Because the silicon die is almost transparent to infrared light, the microscope could focus on the top of the bumps structure and give the temperature with an accuracy of less than 1^{o}C as shown in Figure 6.3. This could be used as a verification tool to check if the results from other methods are valid. Modifications have to be made if multiple samples inside an oven are to be monitored using this tool.

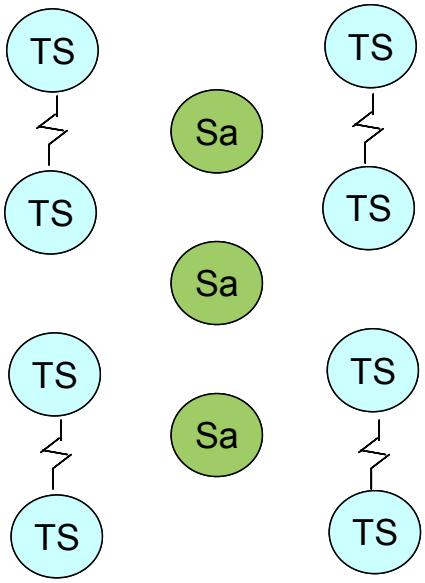


Figure 6.2 Temperature sensor (TS) surrounding the bumps under test (Sa)

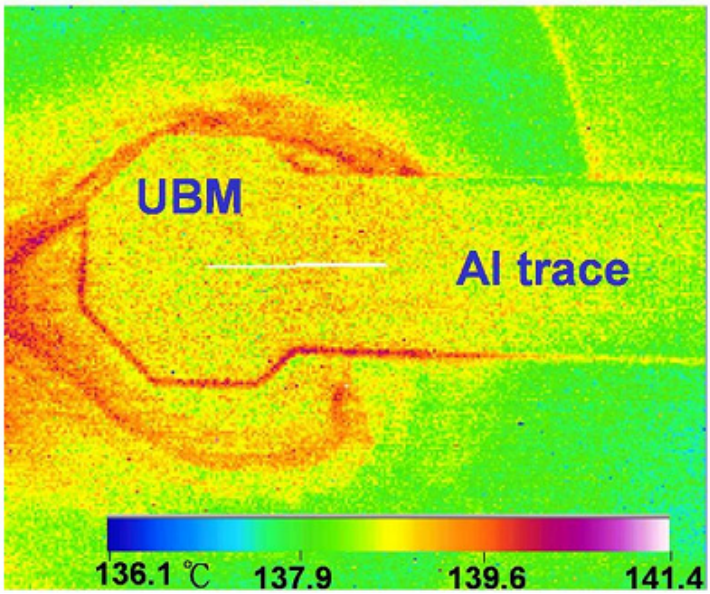


Figure 6.3 Temperature map of solder bump in electromigration test

6.2.2 Current Exponent of Black's Equation

The current exponent, n, of Black's equation is one important parameter to extrapolate the experimental data to realistic lifetime at working conditions. Chae, *et al.* reported the study of current exponent of the Pb-free solder [6.5]. The challenge of getting the correct results also lies in calibrating the Joule heating effect. The difference between lowest and the highest current density in Chae's report was only ~37%. However, the large change in power dissipation (~87%) caused ~7^{o}C difference in between the two samples. Therefore, under the same nominal temperature, higher current density induced even shorter lifetime than expected due the higher actual temperature. This resulted in exceptional high current exponent (2.9~3.5) as shown in Figure 6.4. By correcting the bump temperature using an FEA model, it was found that n was equal to 1.45 and 2.2 for Cu and Ni UBM, respectively.

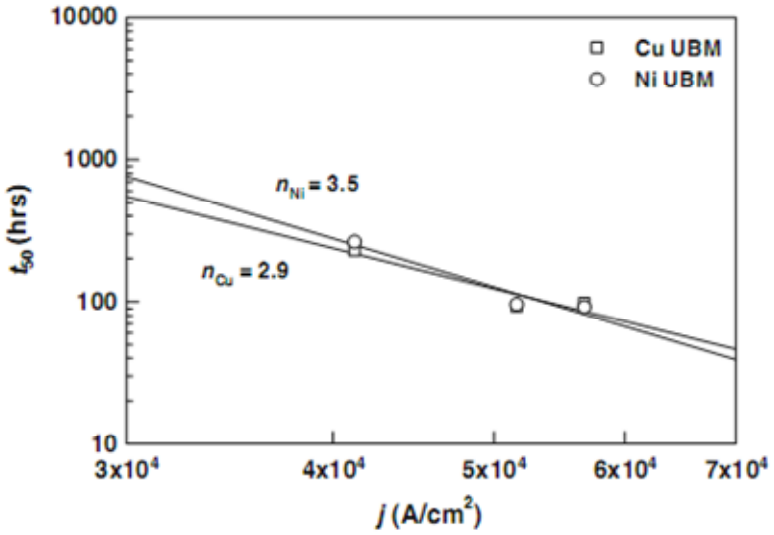


Figure 6.4 Lifetime-current dependency and current exponent deduction

6.2.3 Mechanical Degradation of the Solder Joints

Kirkendall voids have been found to degrade the mechanical strength of the interface involved. As describe in chapter 2, the degradation would be accelerated with electromigration. Zeng, *et al.* studied the Kirkendall void growth by pure thermal aging at the interface between SnAgCu Pb-free solder ball and Cu pad finish on chip scale packages (CSP) [6.6]. This type of packages is widely used in handheld applications such as mobile phones. The CSP package was mounted on to PCB circuit board and then went through a board-level drop test to simulate the mechanical stress it would experience in the field. As can be seen in Figure 6.5, Kirkendall voids appeared after 3 days aging at 125^{o}C and the number of drops that the package could survive dropped ~34% from time zero (Figure 6.6) accordingly. It is expected that the performance will degrade faster if current representative was applied, simulating the working condition of the package.

Therefore, investigating the growth rate and location of the voids with different current density and temperature is of great interest to the handheld device manufacturers.

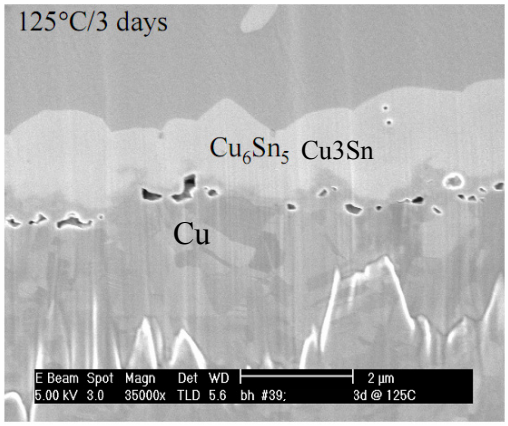


Figure 6.5 Kirkendall voids formed at Cu/Sn interface during thermal aging

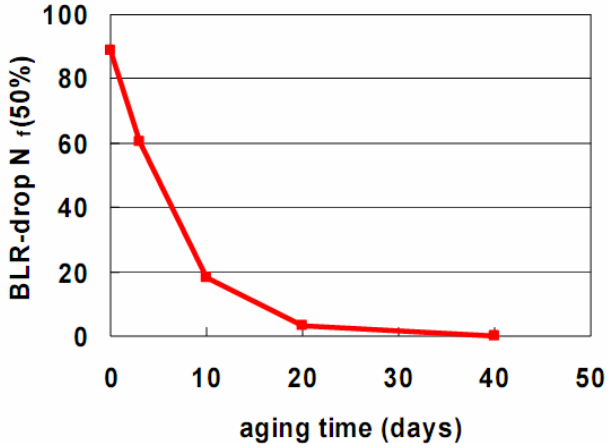


Figure 6.6 Board level drop test performance degradation with thermal aging.

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